



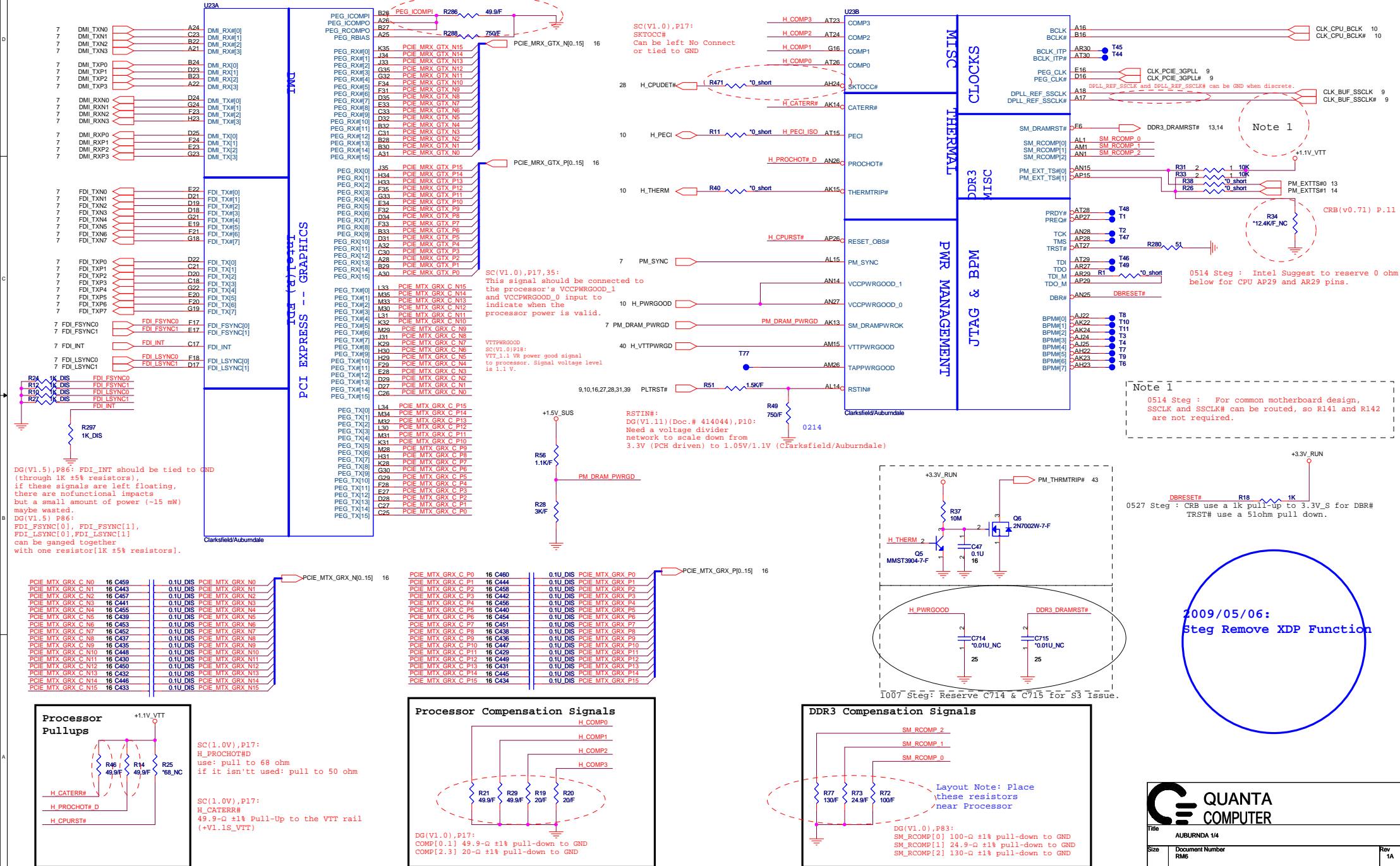
PAGE	DESCRIPTION
1	Schematic Block Diagram
2	Front Page
3-6	Clarksfield/Auburndale
7-12	PCH
13-14	DDRIII SO-DIMM(204P)
15	Clock Generator
16-22	M92-S2-XT
23	BLANK PAGE
24	LCD CONN / HDMI CONN
25	CRT CONN
26	R5U230
27	BLANK PAGE
28	Express/CRard/1394
29	SIO (ITE8502)
30	FLASH / RTC
31	MINI-Card (WWAN)
32	MINI-Card (WLAN/WPAN)
33	Left PUSB/ESATA
34	Right USB
35	SATA (HDD & CD_ROM)
36	TP / KEYBOARD
37	SWITCH / /LED
38	FAN / THERMAL
39	Azelia CODEC
40	AUDIO CONN
41	LAN(RTL8111DL/RJ-45)
42	System Reset Circuit
43	Blank Page
44	1.8V_RUN(RT9018/RT9024)
45	Charger (MAX8731)
46	3V/5V (TPS51427A)
47	1.5_DDR/0.75(TPS51116)
48	1.05V_PCH(TPS51218)
49	1.1_VTT(TPS51218)
50	VGA_M92-XT(MAX8792)
51	CPU CORE(MAX17036)
52	Run Power Switch
53	DCin & Batt
54	PAD & SCREW
55	EMI CAP
56	SMBUS BLOCK
57	THERMAL MAP
58	Power Block Diagram
59	Power sequence Block
60	XDP

Power States

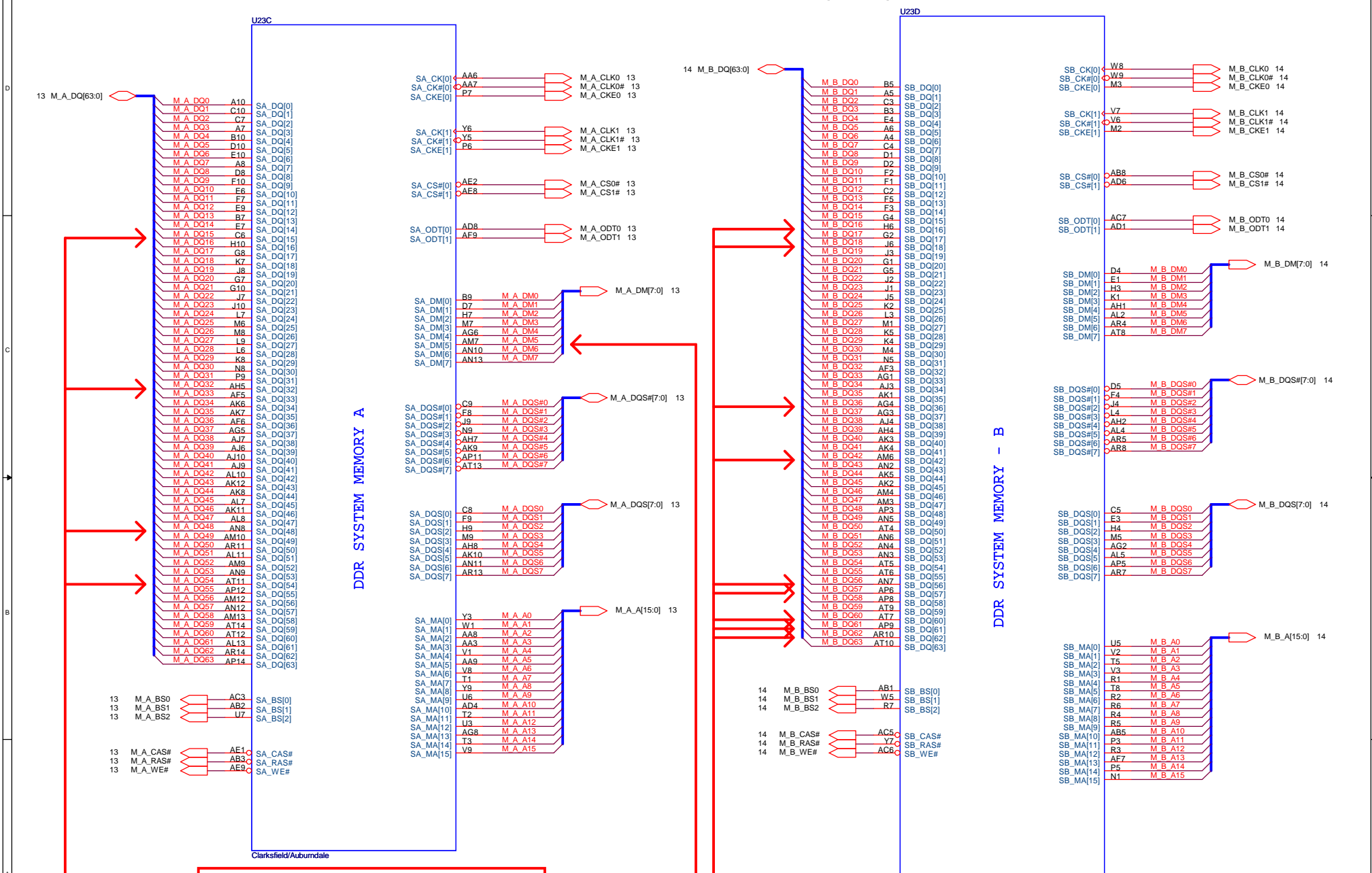
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
+PWR_SRC	10V~+19V	24,30,45,46,47,48,49,50,51	MAIN POWER		S0~S5
+RTC_CELL	+3.0V~+3.3V	08,11,29,30	RTC		S0~S5
+5V_ALW2	+5V	37,46,53	LARGE POWER	MAIN POWER	S0~S5
+5V_ALW	+3.3V	13,33,37,44,46,47,48,49,50,51,52	LARGE POWER	ALW_ON	S0~S5
+3.3V_ALW	+3.3V	29,30,35,36,37,42,44,45,46,47,51,52,53	8051 POWER	3.3V_ALW_ON	S0~S5
+5V_SUS	+5V	11,33,34,37,51,52	SLP_S5# CTRLD POWER	SUS_ON	
+3.3V_SUS	+3.3V	7,09,10,11,13,14,19,24,28,29,37,41,42,44,48,49,50,52	SLP_S5# CTRLD POWER	SUS_ON	
+1.5V_SUS	+1.8V	03,05,13,14,47,50,52	SODIMM POWER	SUS_ON	
+0.75V_DDR_VTT	+0.9V	13,14,47,52	SODIMM POWER	RUN_ON	
+5V_RUN	+5V	11,18,24,25,35,36,38,39,40,51,52	SLP_S3# CTRLD POWER	RUN_ON	
+3.3V_RUN	+3.3V	3,7,8,9,10,11,13,14,15,17,24,25,26,28,29,30,31,32,33,35,37,38,39,40,41,42,46,51,52,59,60	SLP_S3# CTRLD POWER	RUN_ON	
+1.8V_RUN	+1.8V	05,11,44,52	SDVO POWER	RUN_ON	
+1.8V_RUN_GFX	+1.25V	17,18,21,22,44,52	VGA POWER	RUN_ON	
+1.5V_RUN	+1.5V	11,18,19,20,28,31,32,52	CALISTOGA/ICH9 POWER	RUN_ON	
+VCC_GFX_CORE	+0.9V~+1.2V	18,21,50	VGA POWER	RUN_ON	
+1.05V_PCH	+1.05V	08,09,11,15,48	CPU/CALISTOGA/ICH8 POWER	1.05V_RUN_ON	
+VCC_CORE	+0.7V~+1.77V	05,51	CPU CORE POWER	IMVP_VR_ON	
+LCDVCC	+3.3V	26	LCD Power	LCDVCC_TST_EN & ENVDD	
+5V_MOD	+5V	36	Module Power	MODC_EN	
+5V_HDD	+5V	36	HDD Power	HDDC_EN	
+1.1V_VTT	+1.1V	03,05,10,11,49,59			
+1.1V_GFX_PCIE	+1.1V	18,50			

GND PLANE	PAGE	DESCRIPTION
⏏ GND_CHG	46	
⏏ GND_1.05V	47	
⏏ GND_VGA	50	
⏏ GND_SIGNAL	51	
⏏ AGND_DC/DC	52	
⏏ GND	ALL	

SC(V1.0),P11: Should be shorted at the pins and then routed to one end of the 49.9-Q $\pm 1\%$ resistor, pulled-down to GND on the board.



AUBURNDALE/CLARKSFIELD PROCESSOR (DDR3)



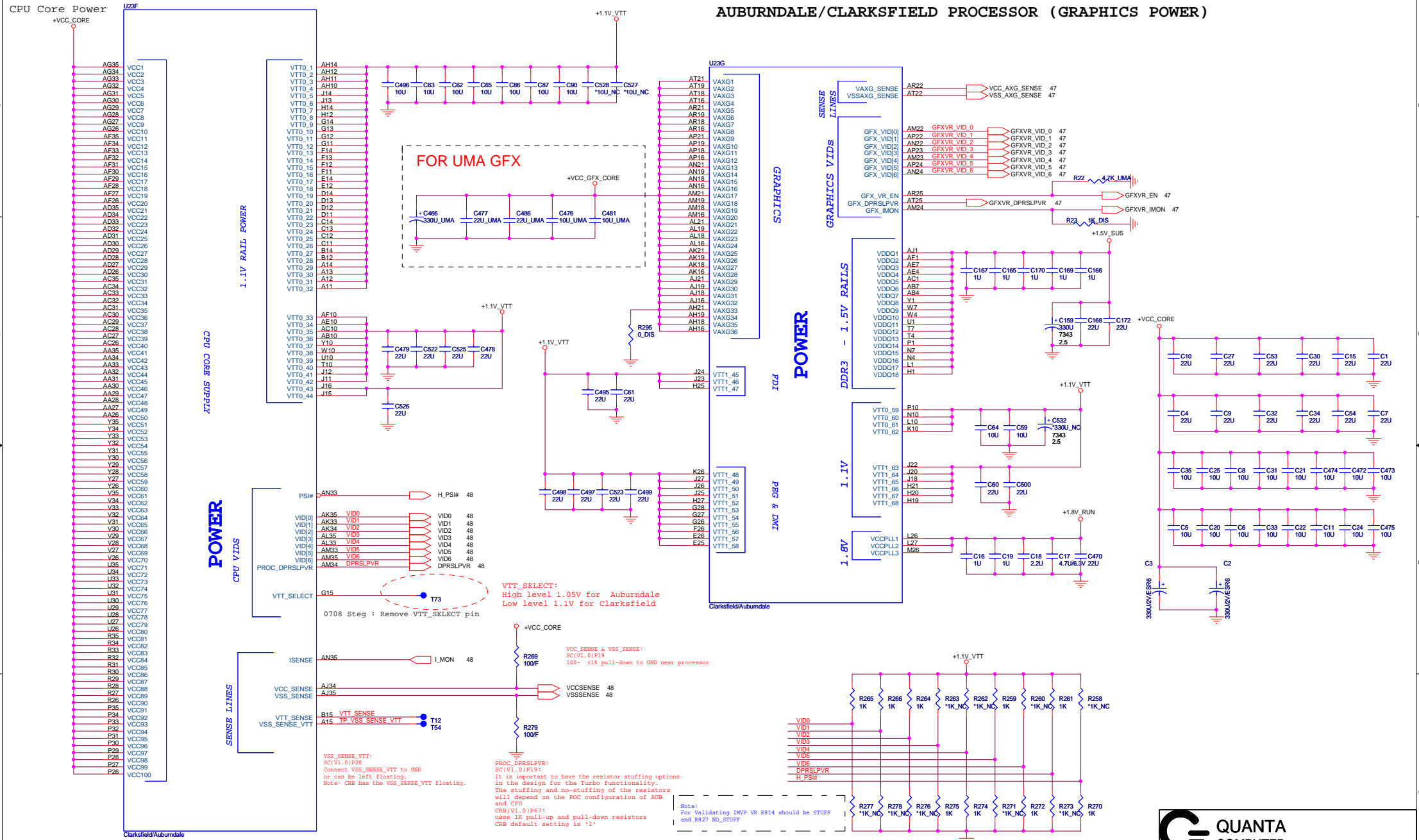
Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

**QUANTA
COMPUTER**

Title AUBURNDA 2/4		
Size RM6	Document Number	Rev 1A
Date: Thursday, October 08, 2009	Sheet 4	of 62

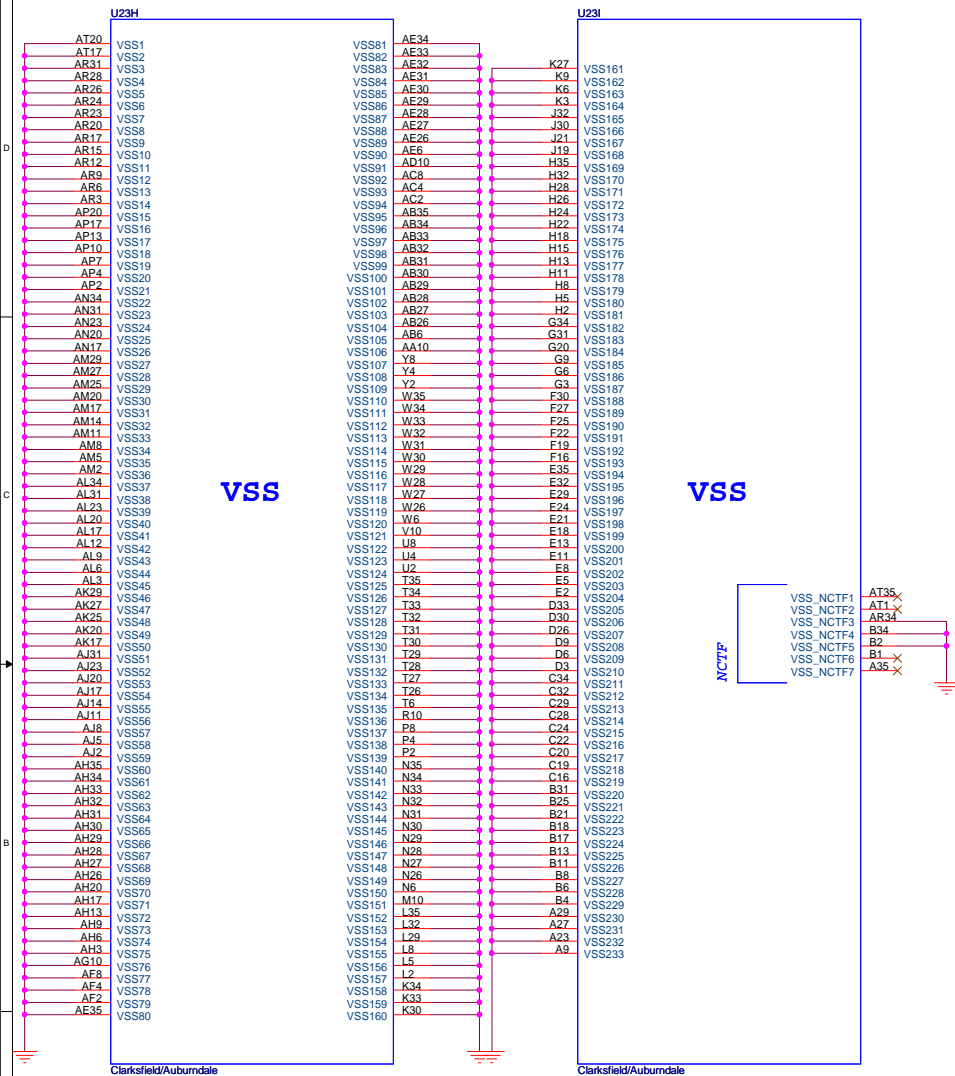
AUBURNDALE/CLARKSFIELD PROCESSOR (GRAPHICS POWER)



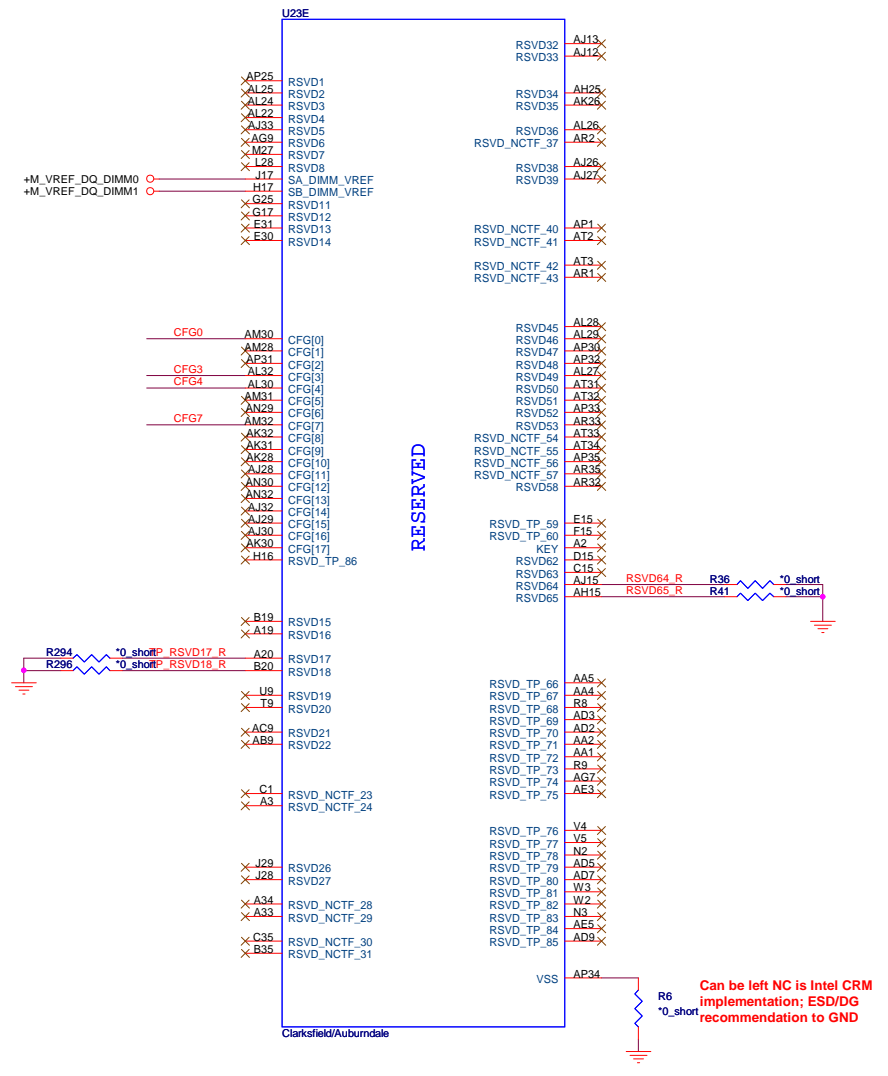
AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

0525 Step: As an option, VTT_SENSE pin on the processor can be left floating. But the platform needs to have the FB (feedback) pin of the VR tied to the VTT plane regulation.

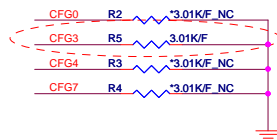
AUBURNDALE/CLARKSFIELD PROCESSOR (GND)



AUBURNDALE/CLARKSFIELD PROCESSOR(RESERVED, CFG)



The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Display Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

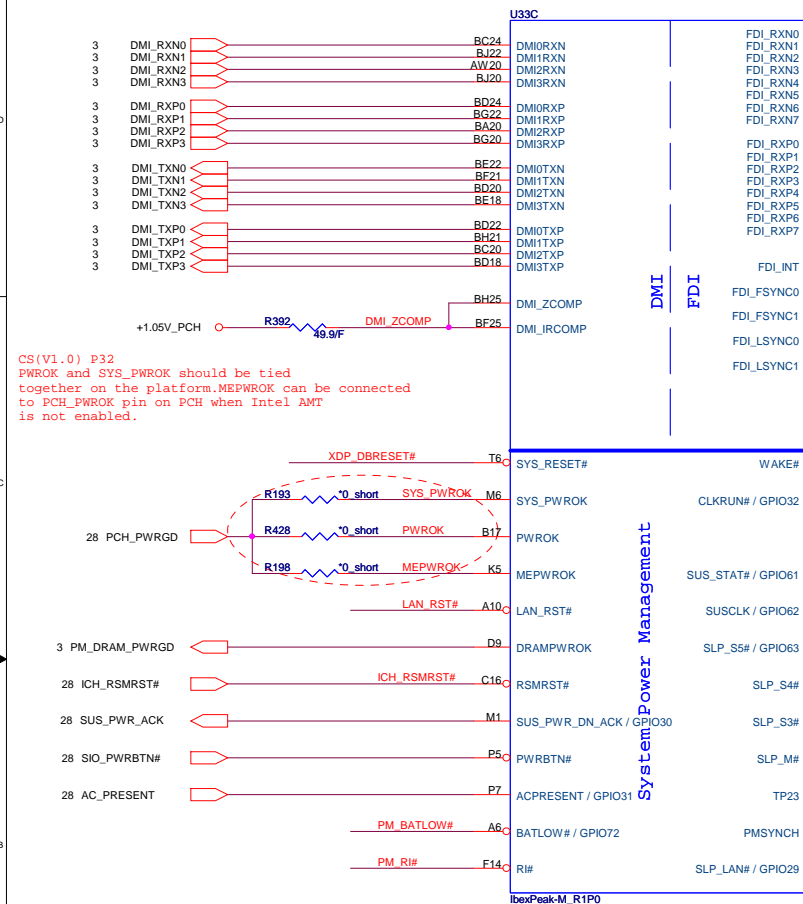
QUANTA
COMPUTER

Title: AUBURND 4/4

Size: Document Number RM6 Rev 1A

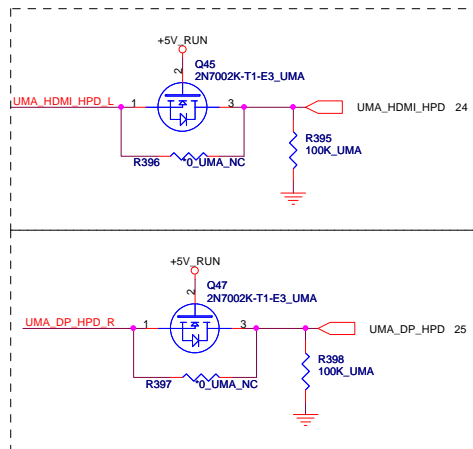
Date: Thursday, October 08, 2009 Sheet 6 of 62

IBEX PEAK-M (DMI, FDI, GPIO)

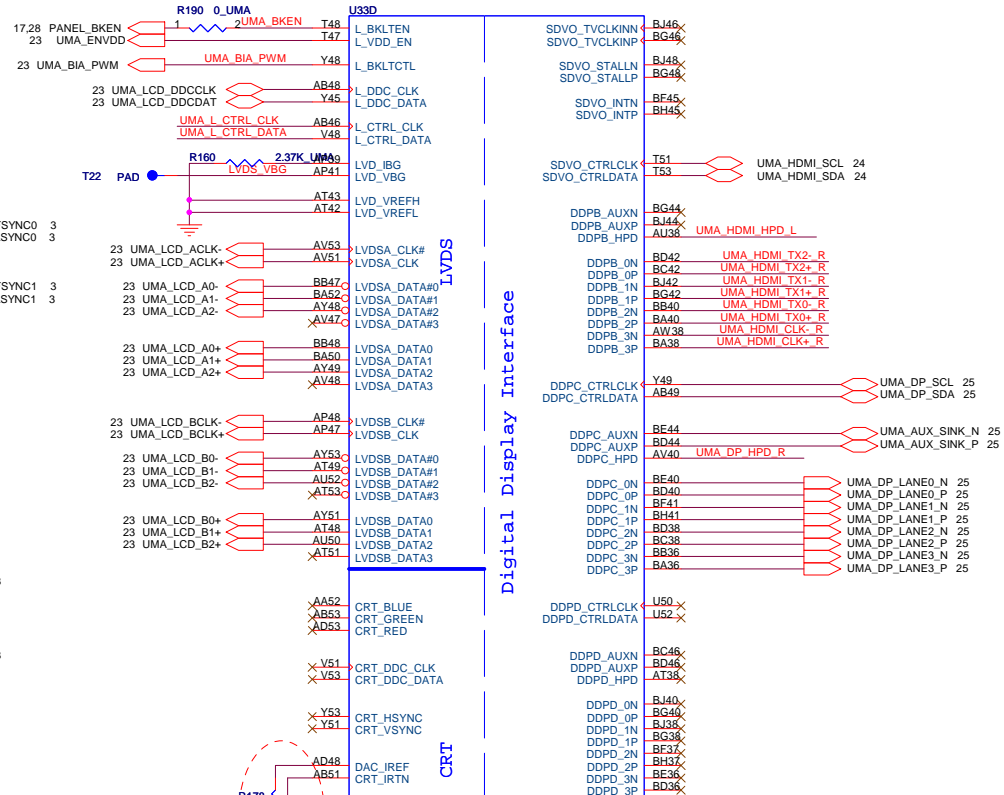


CS(V1.0) P32
PWROK and SYS_PWROK should be tied together on the platform. MEPWROK can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.

MEPWROK
SC(V1.0) P32:
It can be connected to PCH_PWROK pin on PCH when Intel AMT is not enabled.



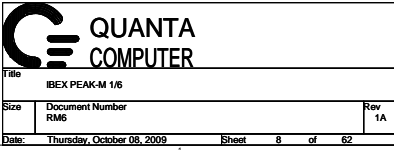
IBEX PEAK-M (LVDS, DDI)



UMA HDMI TX2+ R	C337	0.1U UMA	UMA_HDMI_TX2+ 24
UMA HDMI TX2+ R	C336	0.1U UMA	UMA_HDMI_TX2+ 24
UMA HDMI TX1+ R	C330	0.1U UMA	UMA_HDMI_TX1+ 24
UMA HDMI TX1+ R	C331	0.1U UMA	UMA_HDMI_TX1+ 24
UMA HDMI TX0+ R	C324	0.1U UMA	UMA_HDMI_TX0+ 24
UMA HDMI TX0+ R	C325	0.1U UMA	UMA_HDMI_TX0+ 24
UMA HDMI CLK+ R	C329	0.1U UMA	UMA_HDMI_CLK+ 24
UMA HDMI CLK+ R	C328	0.1U UMA	UMA_HDMI_CLK+ 24



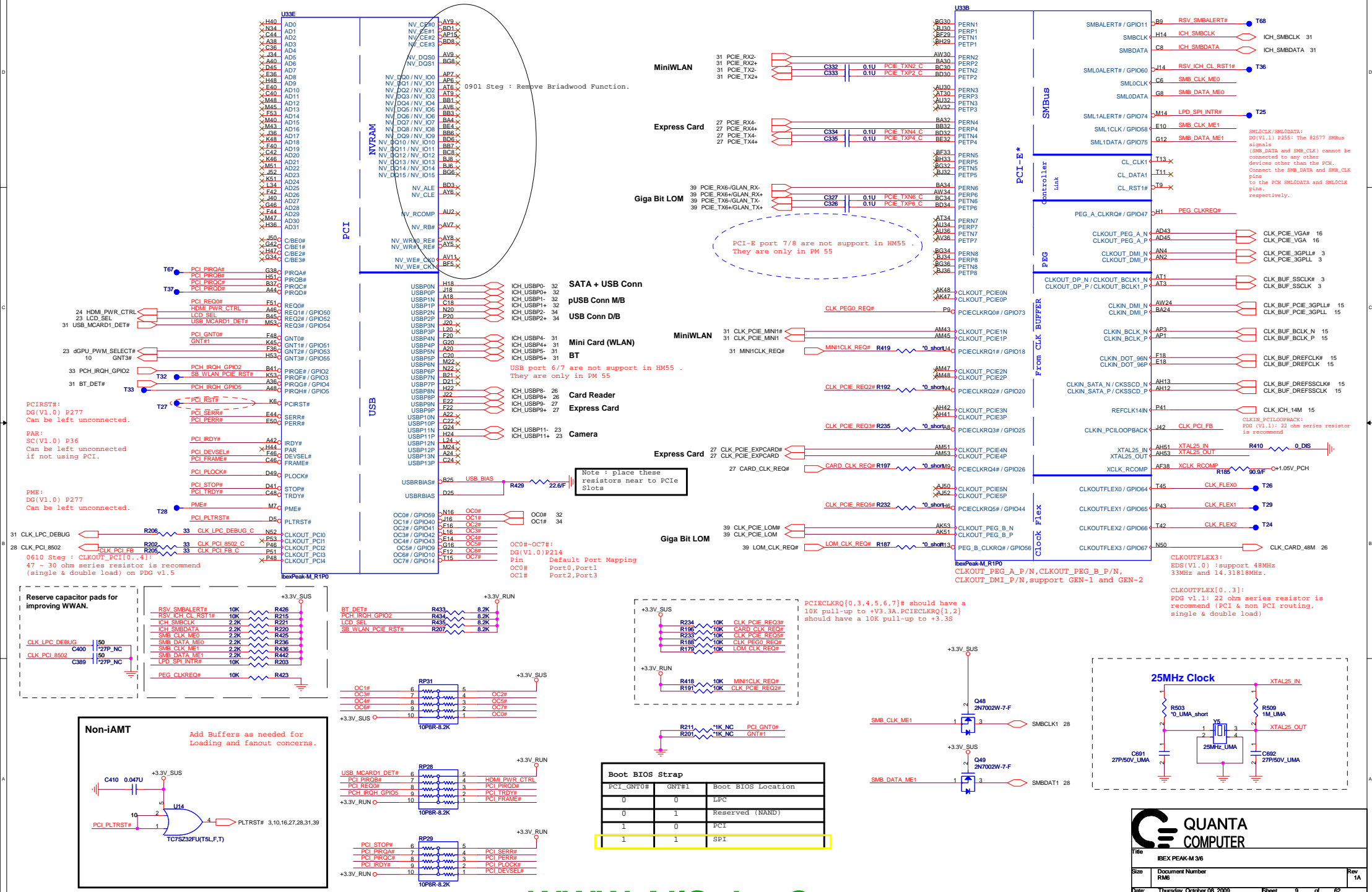
Title			IBEX PEAK-M 2/6
Size	Document Number	Rev	
	RM6	1A	
Date:	Thursday, October 08, 2009	Sheet	7 of 62



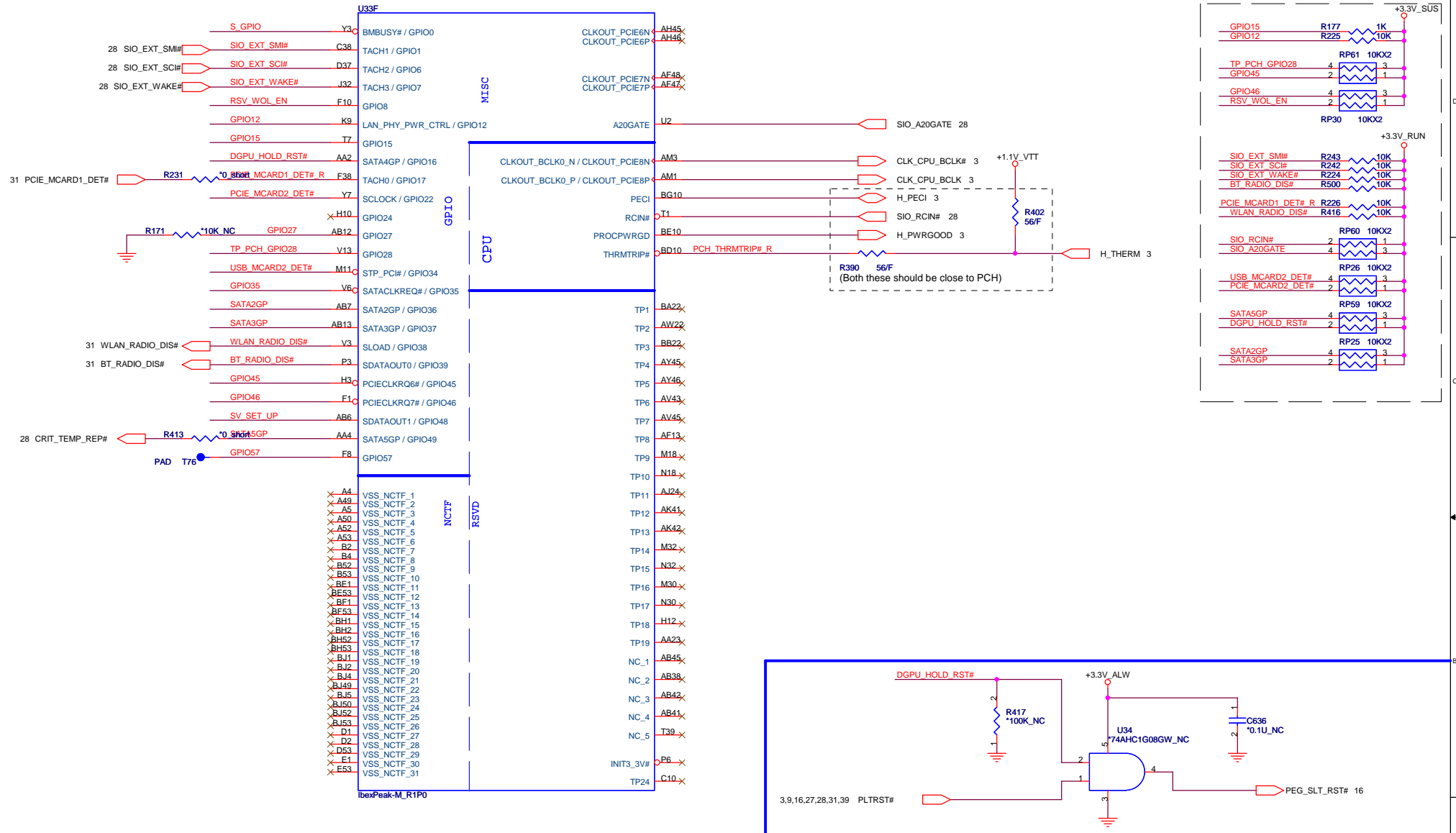
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

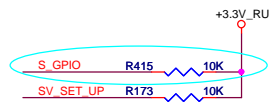


IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN	Enable when sampled low Disable when sampled high



SV_SET_UP	1-X High = Strong (Default)
-----------	-----------------------------

6

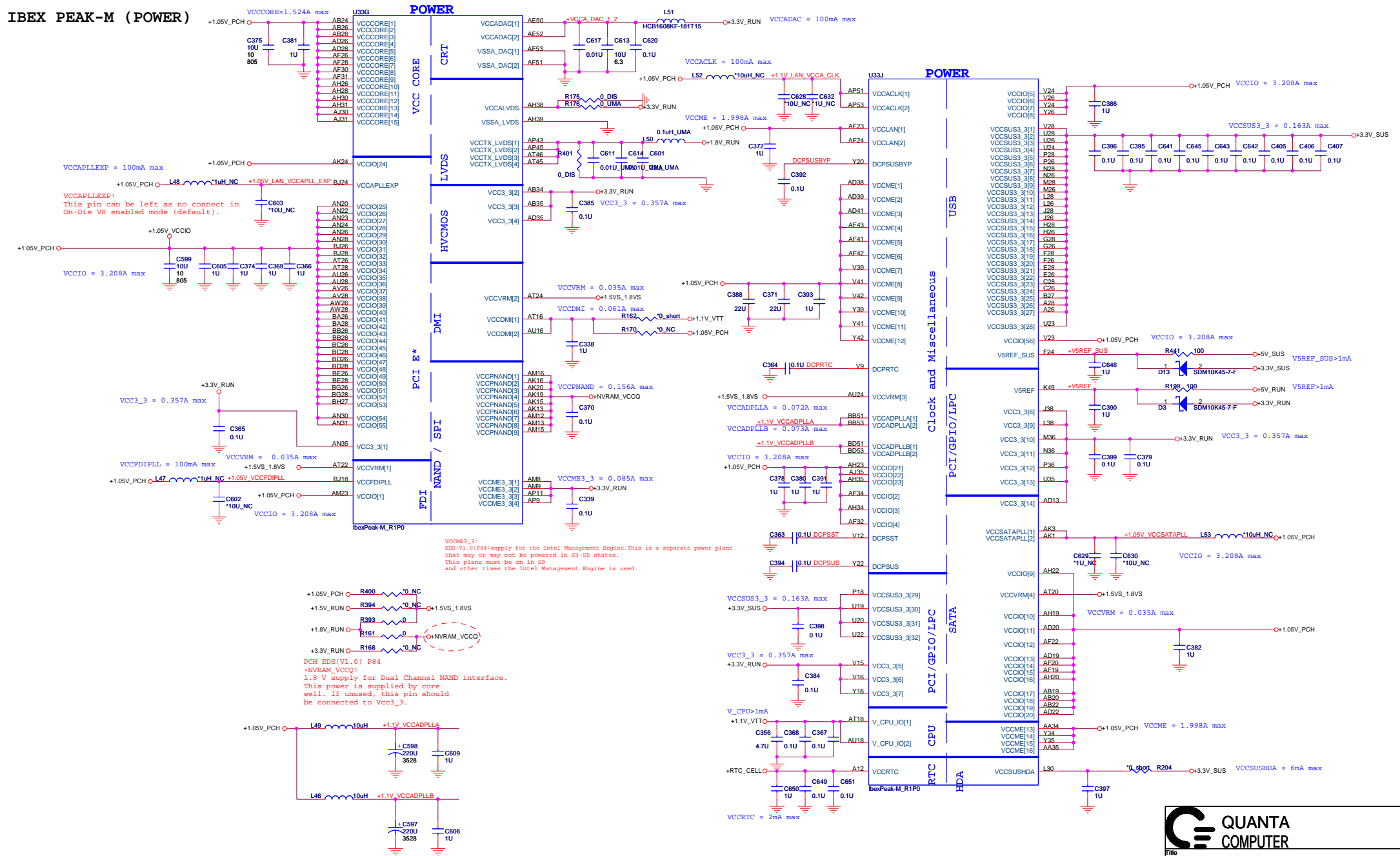
BMBUSY#:
If not used, require a weak pull-up (8.2~ 10k to Vcc3.3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.



Title IBEX PEAK-M 4/6			
Size	Document Number RM6	Rev 1A	
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IBEX PEAK-M (POWER)



Title	IBEX PEAK-M 5/6
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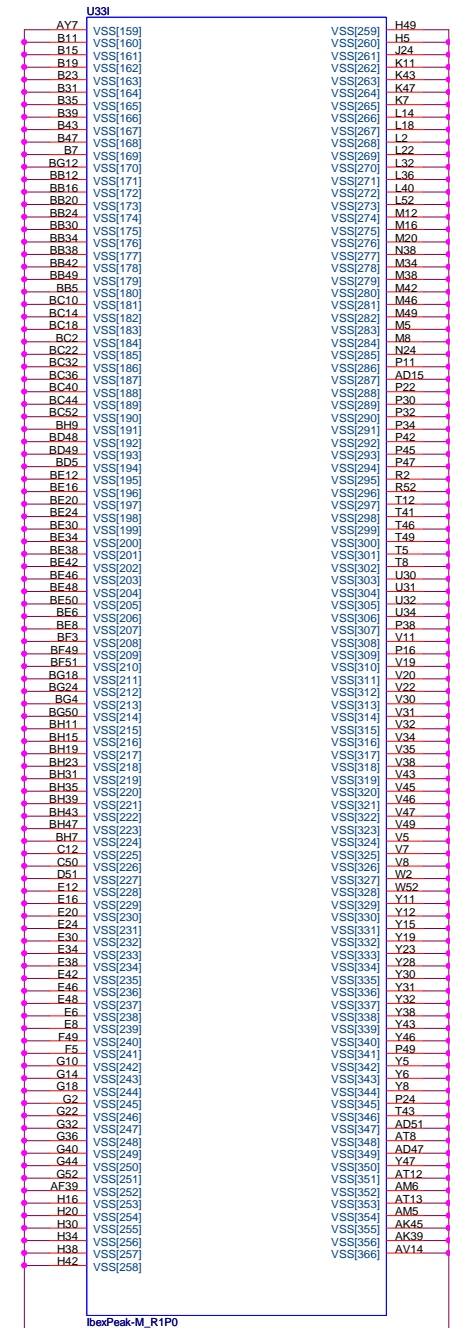
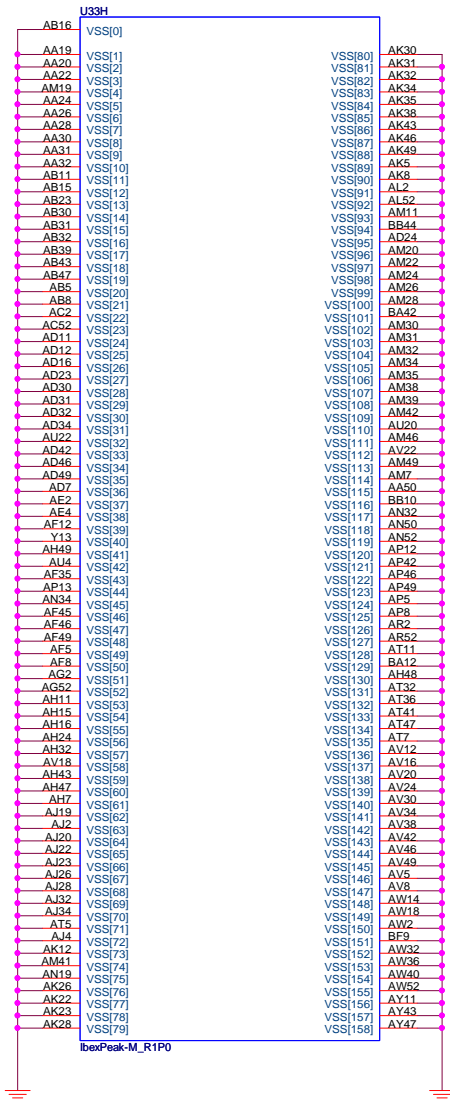
Size	Document Number RM6
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Date: Thursday, October 08, 2009 Sheet 11 of 62

Date: Thursday, October 08, 2009 Sheet 11 of 62

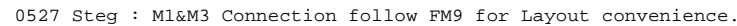
Date: Thursday, October 08, 2009 Sheet 11 of 62

IBEX PEAK-M (GND)



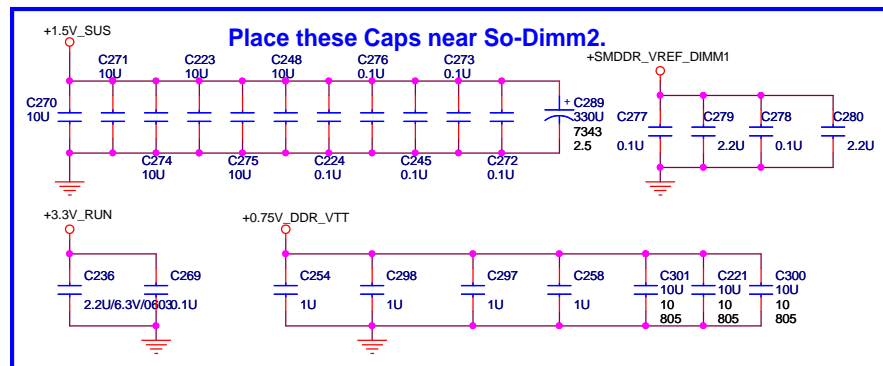
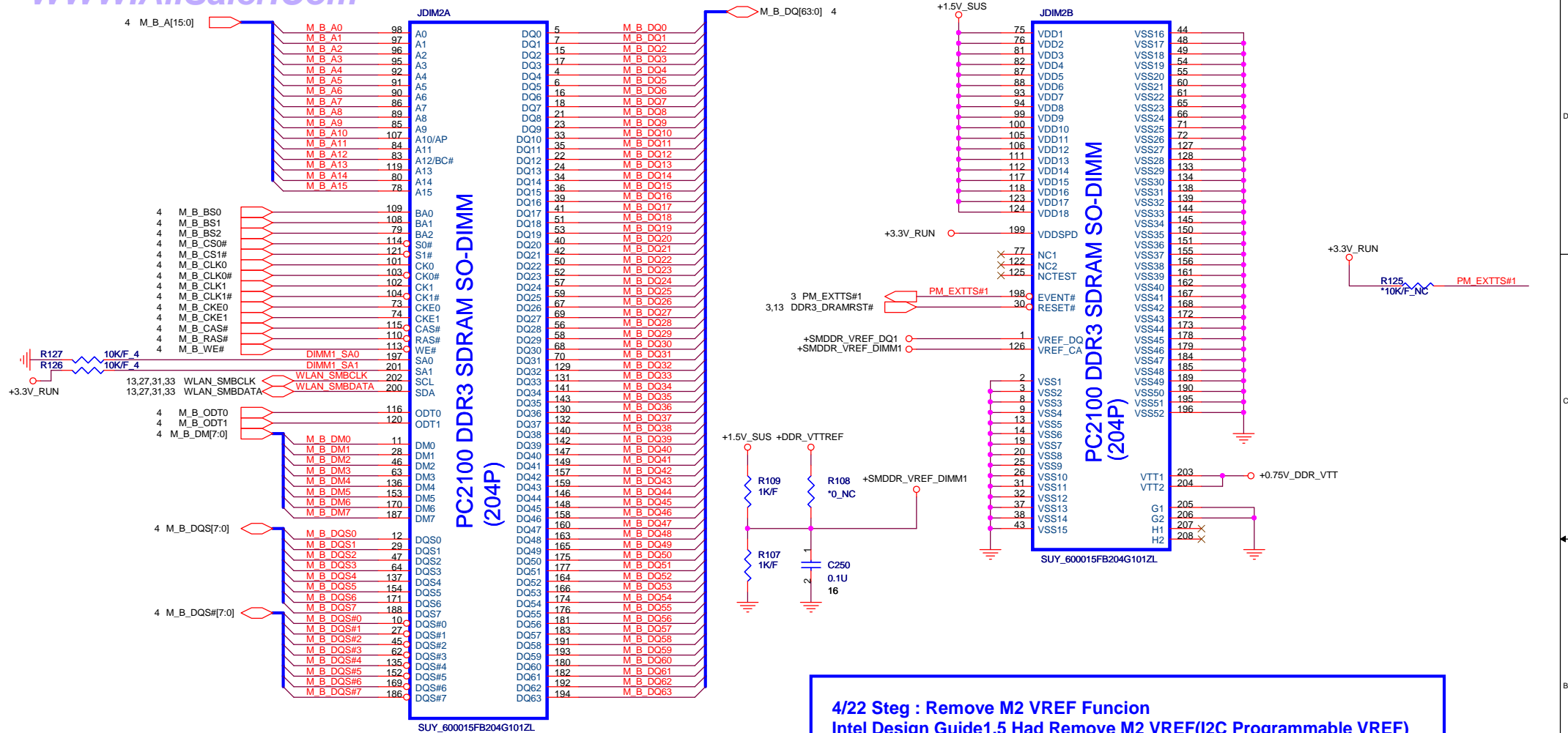
QUANTA
COMPUTER

Title IBEX PEAK-M 6/6		
Size RM6	Document Number RM6	Rev 1A
Date: Thursday, October 01, 2009	Sheet 12	of 62

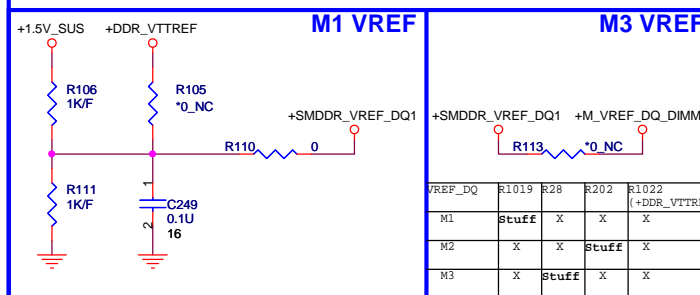


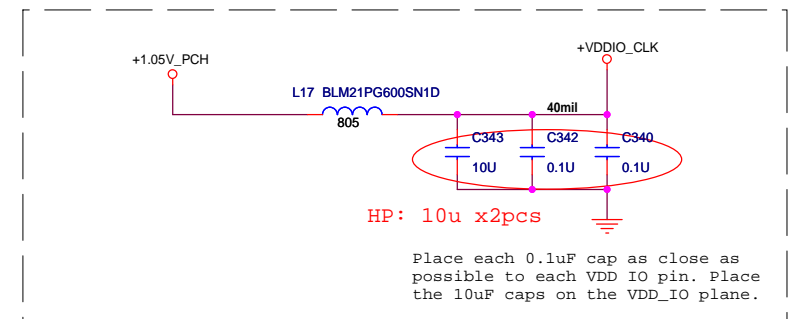
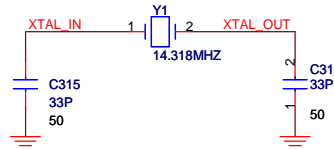
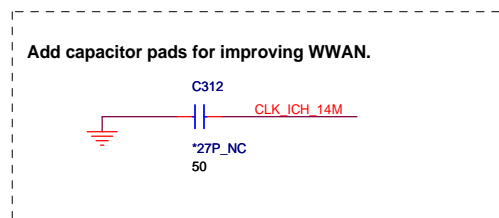
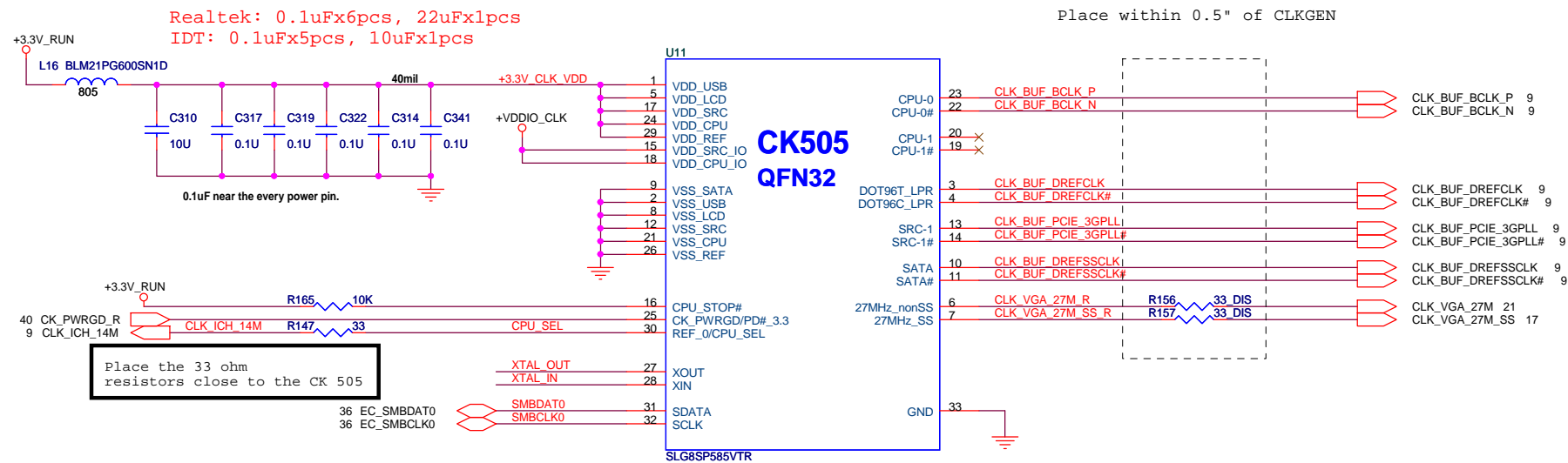
VREF_DQ	R25	R24	R204	R1018 (+DDR_VITRE
M1	Stuff	X	X	X
M2	X	X	Stuff	X
M3	X	Stuff	X	X

Size	Document Number RM6
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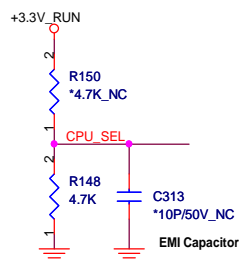


0527 Steg : M1&M3 Connection follow FM9 for Layout convenience.



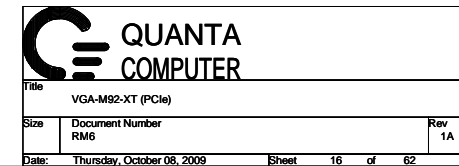


+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V, Max 3.465V.
Realtek date sheet (V1.2) P11: Min 1.05V, Max 3.3V.
IDT date sheet (V0.7) P10: Min 0.9975V, Max 3.465V.

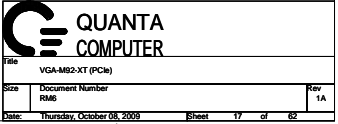


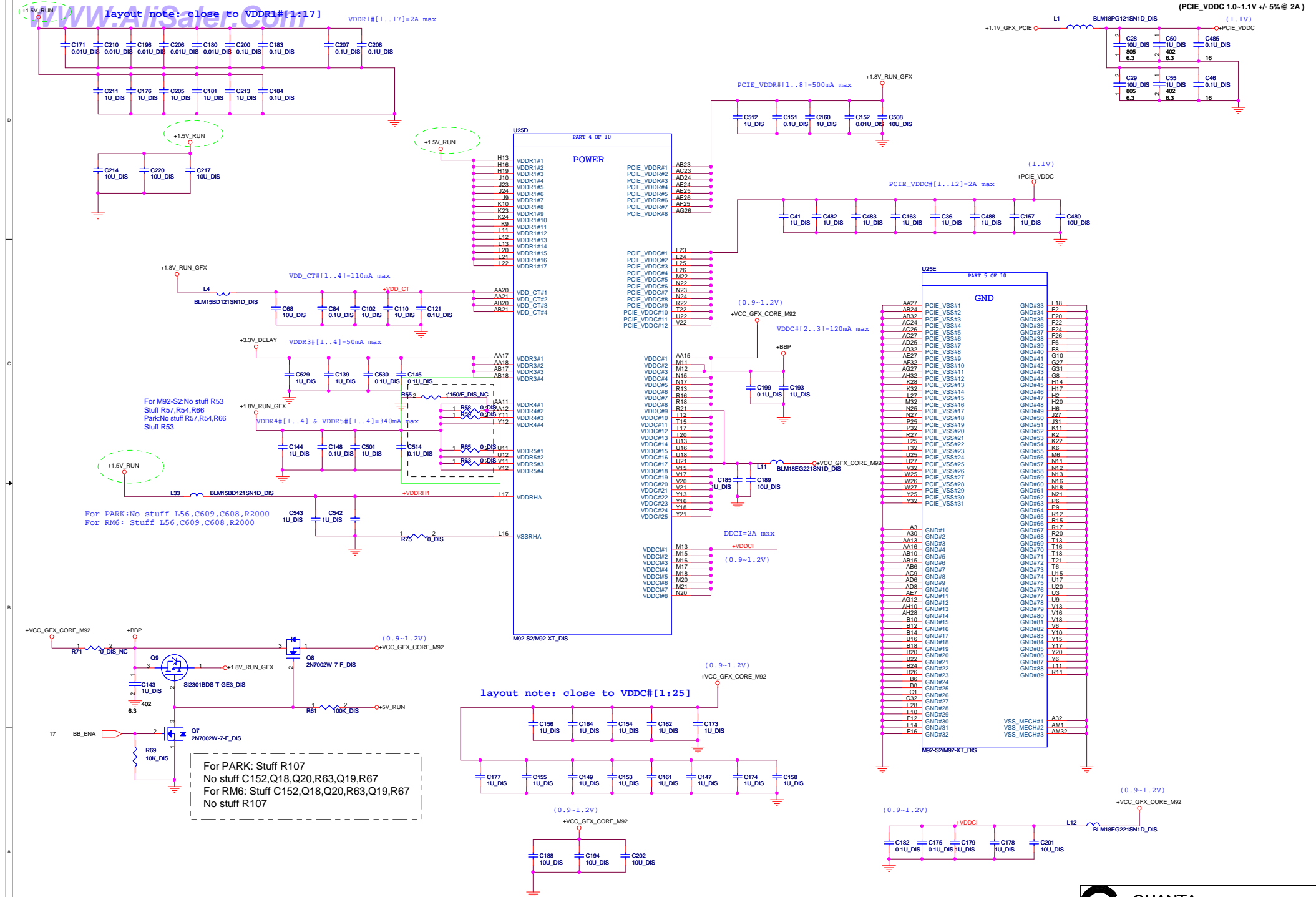
PIN	CPU_0	CPU_1
30		
0 (default)	133MHz	133MHz
1 (0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet (V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet (V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.



Memory Straps	RAM TYPE _CFG2	RAM TYPE _CFG1	RAM TYPE _CFG0	Quanta PN (QuantaBuy)	Quanta PN (WinBuy)	Vendor PN	3l level PN
800MHz 512MB(64M*16) Samsung	0	0	1	AKD5LGGTS02		K4W1G1646S-HC12	
800MHz 512MB(64M*16) Hynix	0	1	0	AKD5LZGTW00		H5TQ1G63BFR-12C	





Title	VGA-M92-XT (PCIe)
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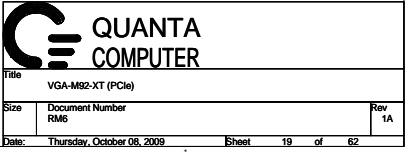
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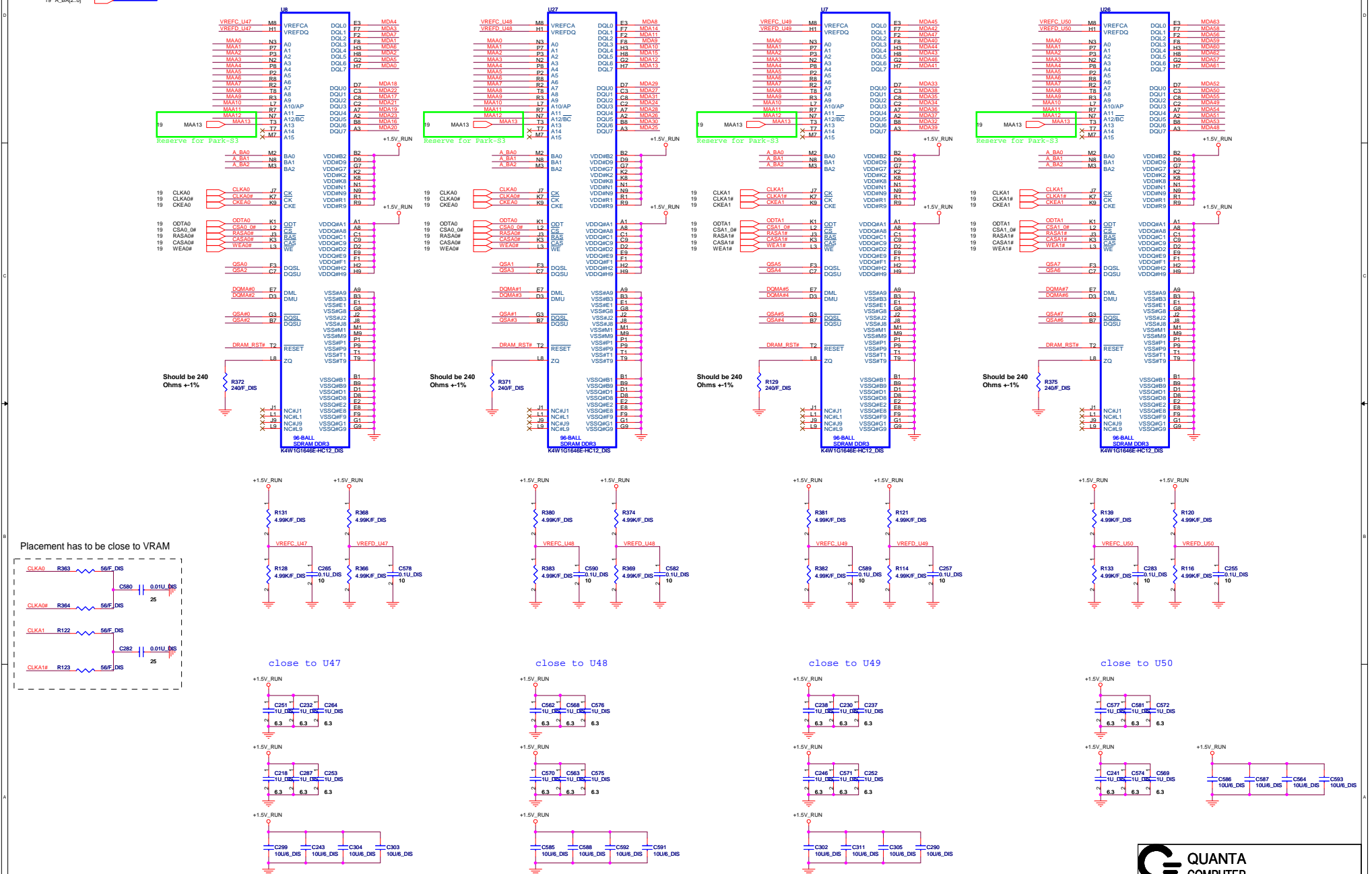
RM6

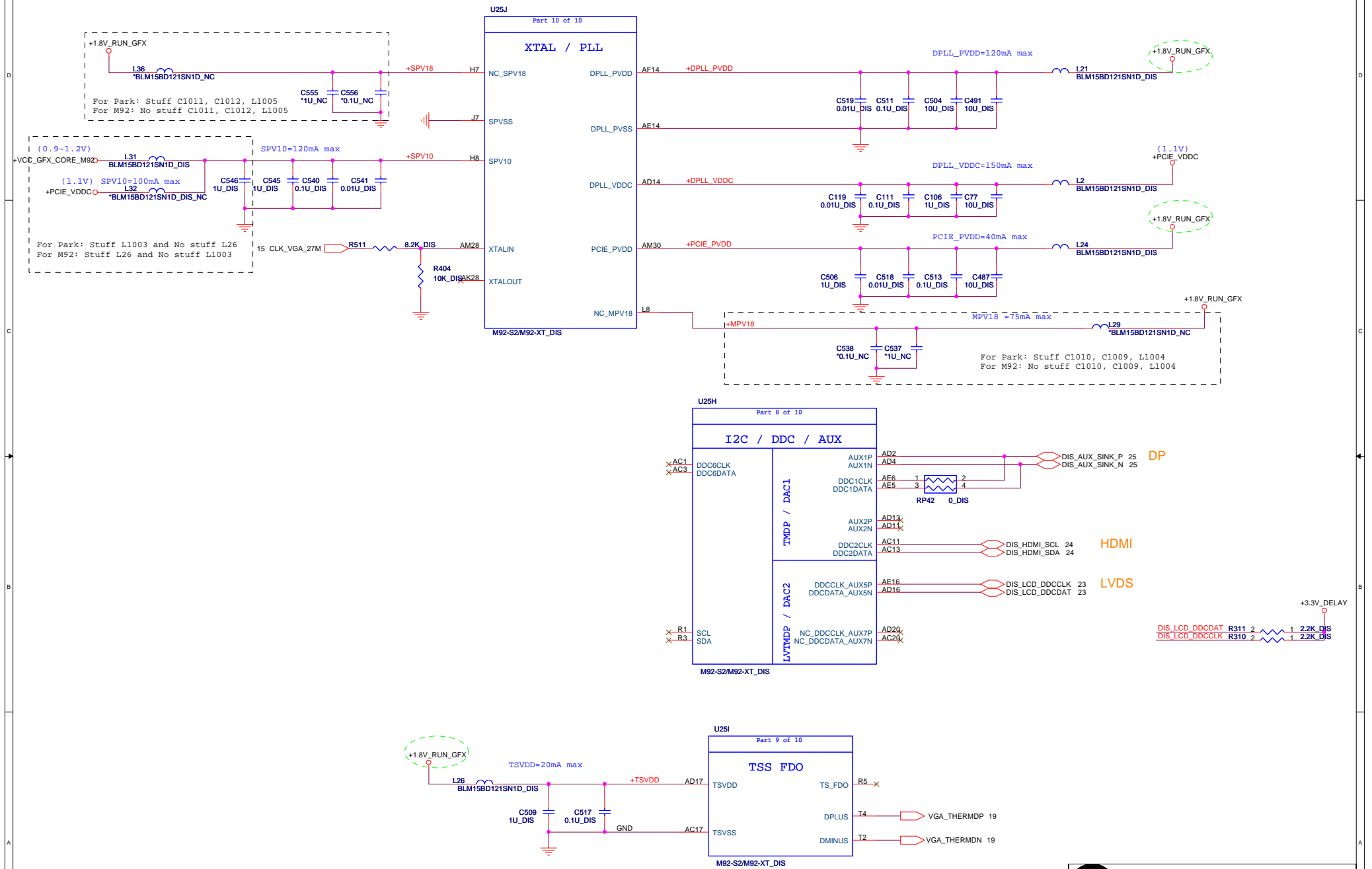
Date: Thursday, October 0

Rev

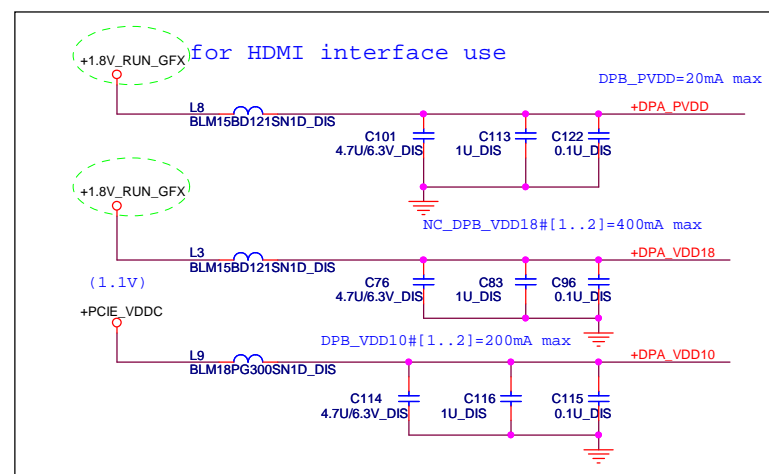
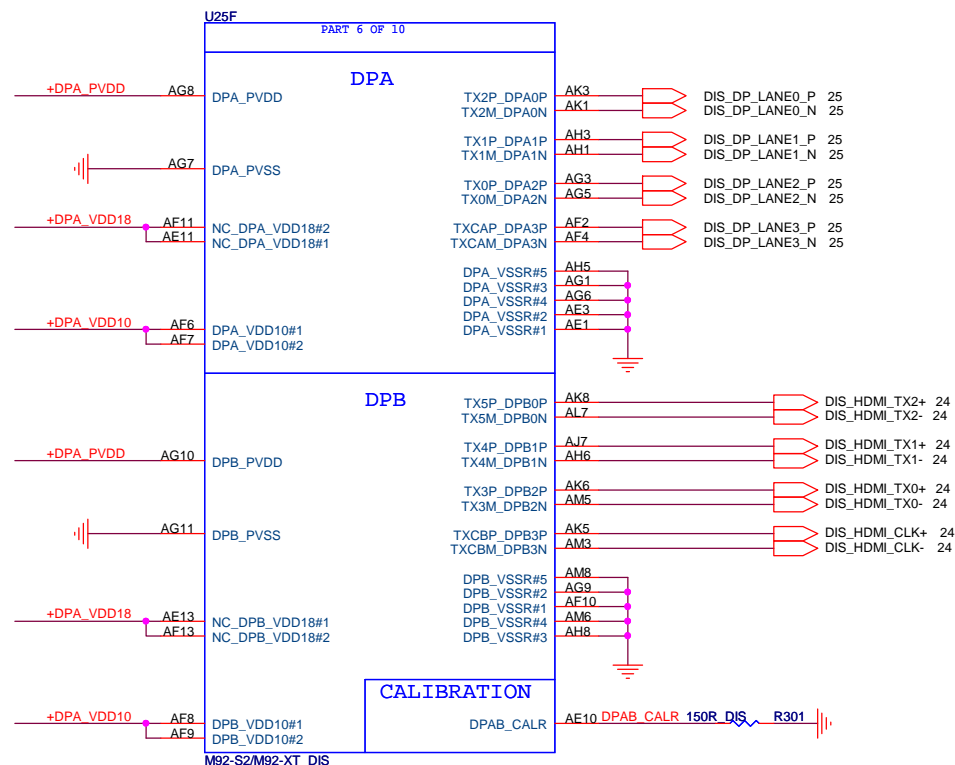
WWW.AliSaler.Com



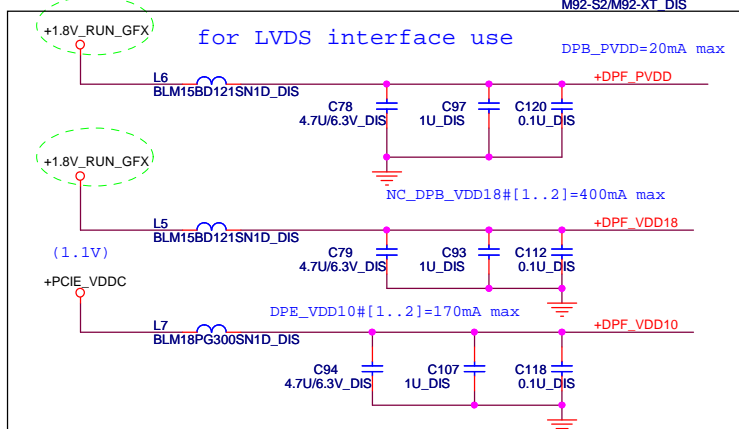
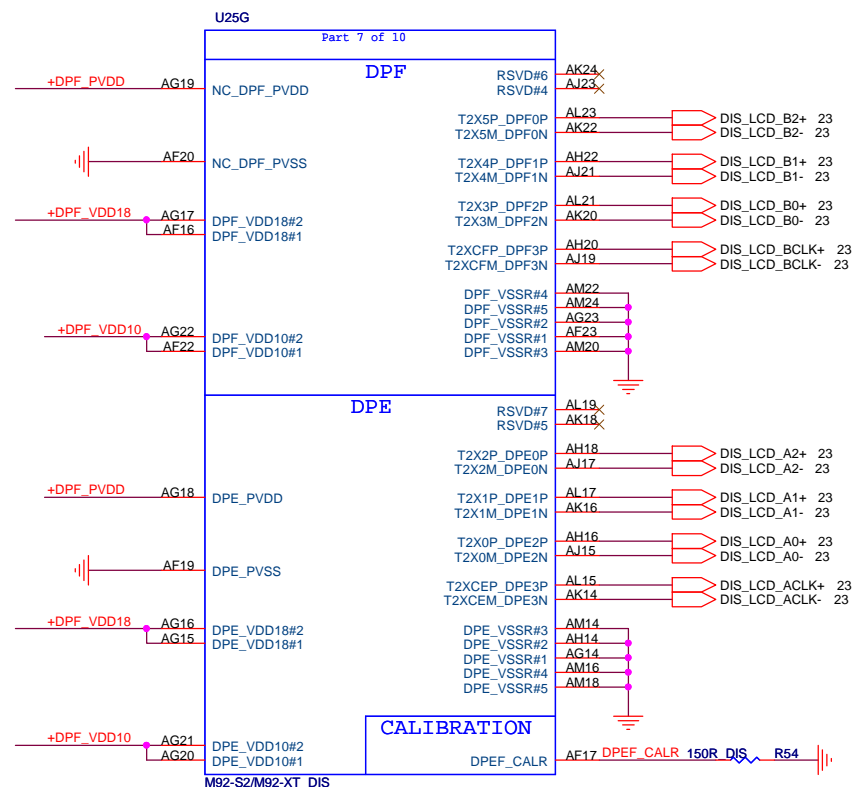




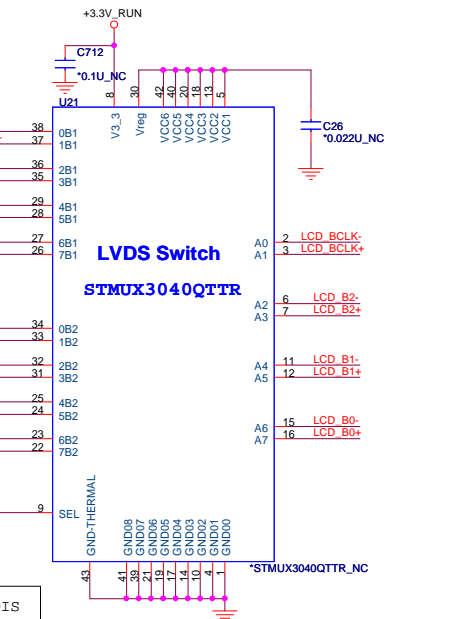
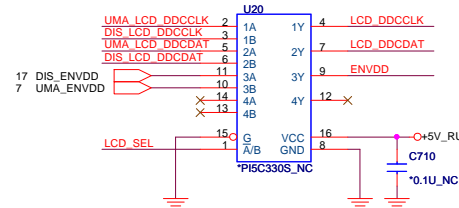
TMDP(HDMI) INTERFACE



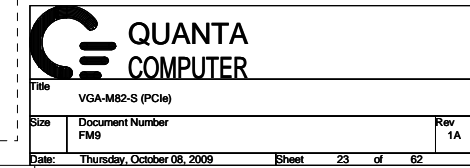
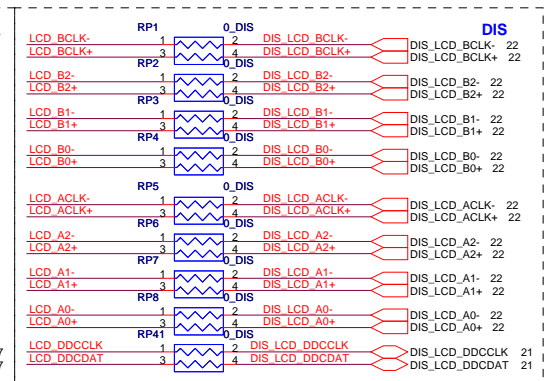
LVDS INTERFACE

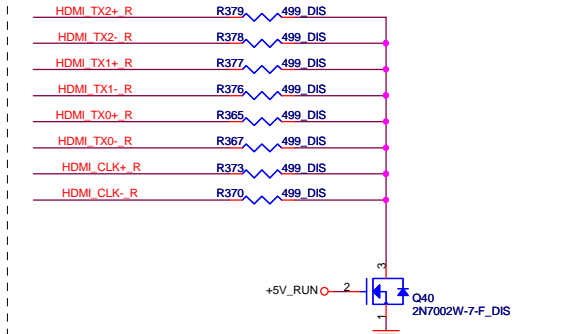
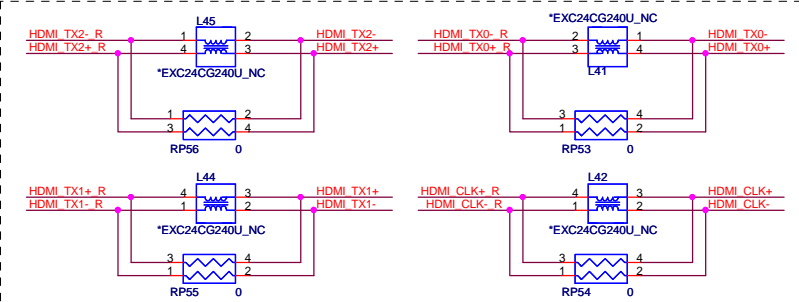
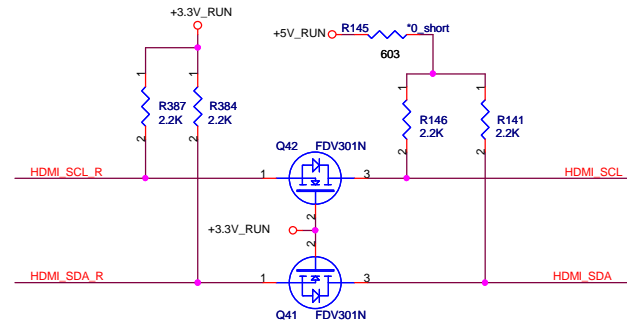
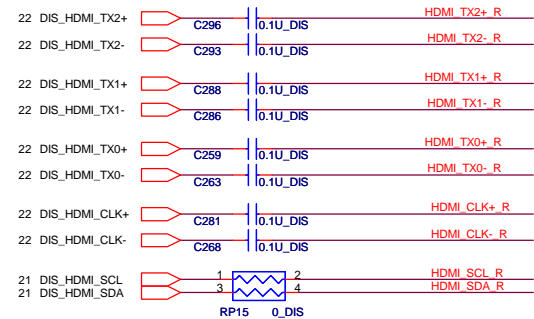


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Title: VGA-M92-XT (PCIe)		
Size: RM6	Document Number: RM6	Rev: 1A
Date: Thursday, October 08, 2009	Sheet: 22	of 62

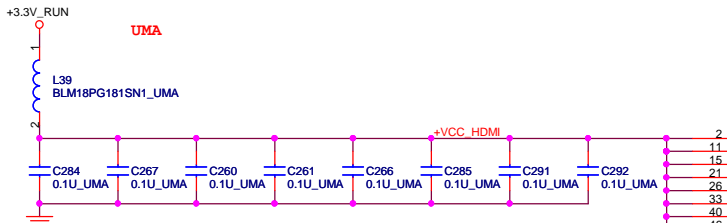
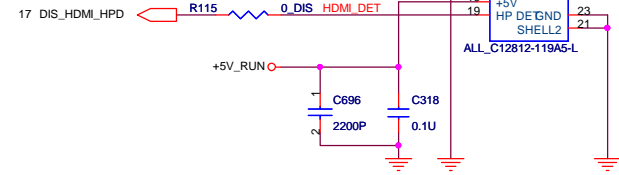
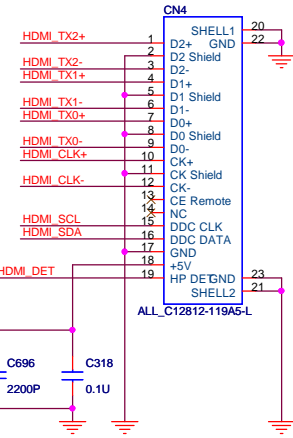


40Pin LVDS & Array Microphone & Camera Connector



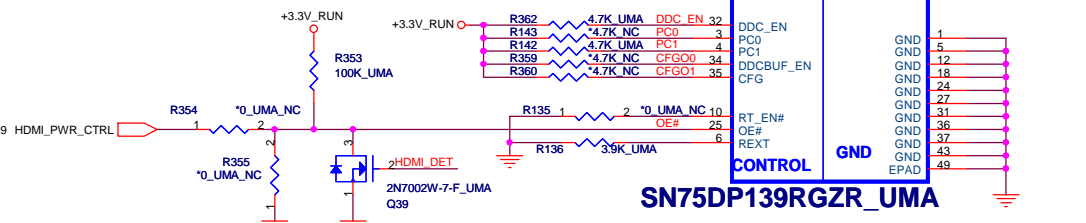
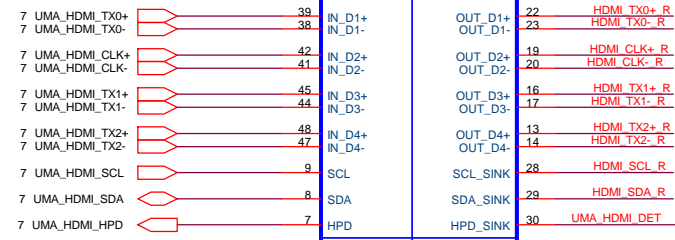


HDMI



EQUALIZATION SETTING
 PC1:PC0=0:0 8dB
 PC1:PC0=0:1 4dB Recommended
 PC1:PC0=1:0 12dB
 PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
 CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
 CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
 CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
 CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V



0827 - CHANGE
 FOR PIM Vender suggests
 R386 : add 0 ohm short to Gnd
 R388 : remove (open)

QUANTA COMPUTER

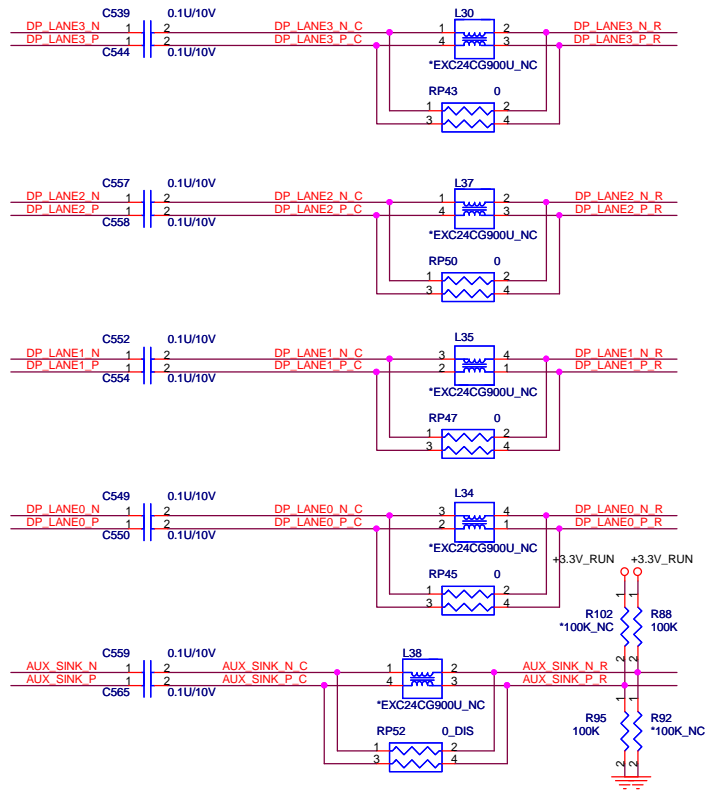
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Size: Document Number

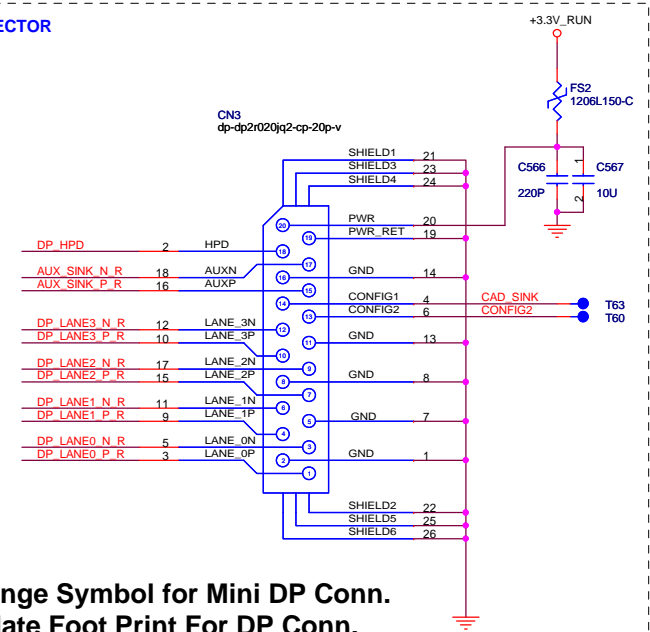
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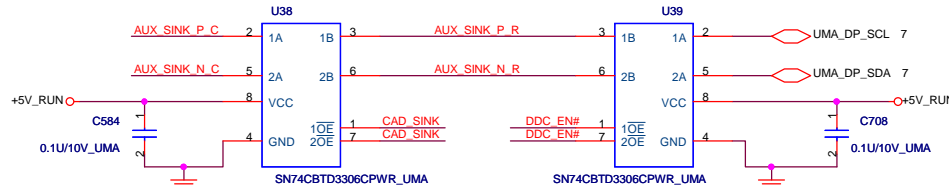
Rev: 1A



MINI DISPLAY PORT CONNECTOR

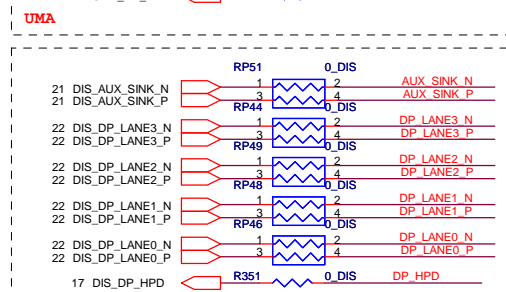
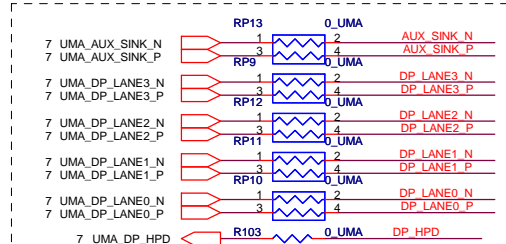
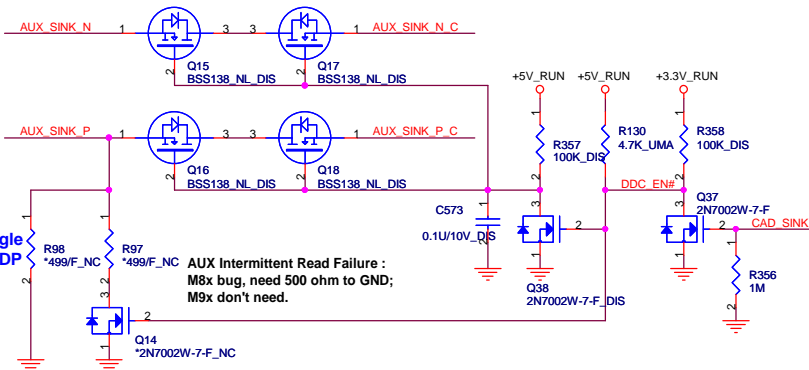


7/28 Steg: Change Symbol for Mini DP Conn.
5/18 Steg: Update Foot Print For DP Conn.

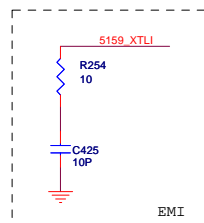


Temporary DP dongle
support circuit for DP
function test

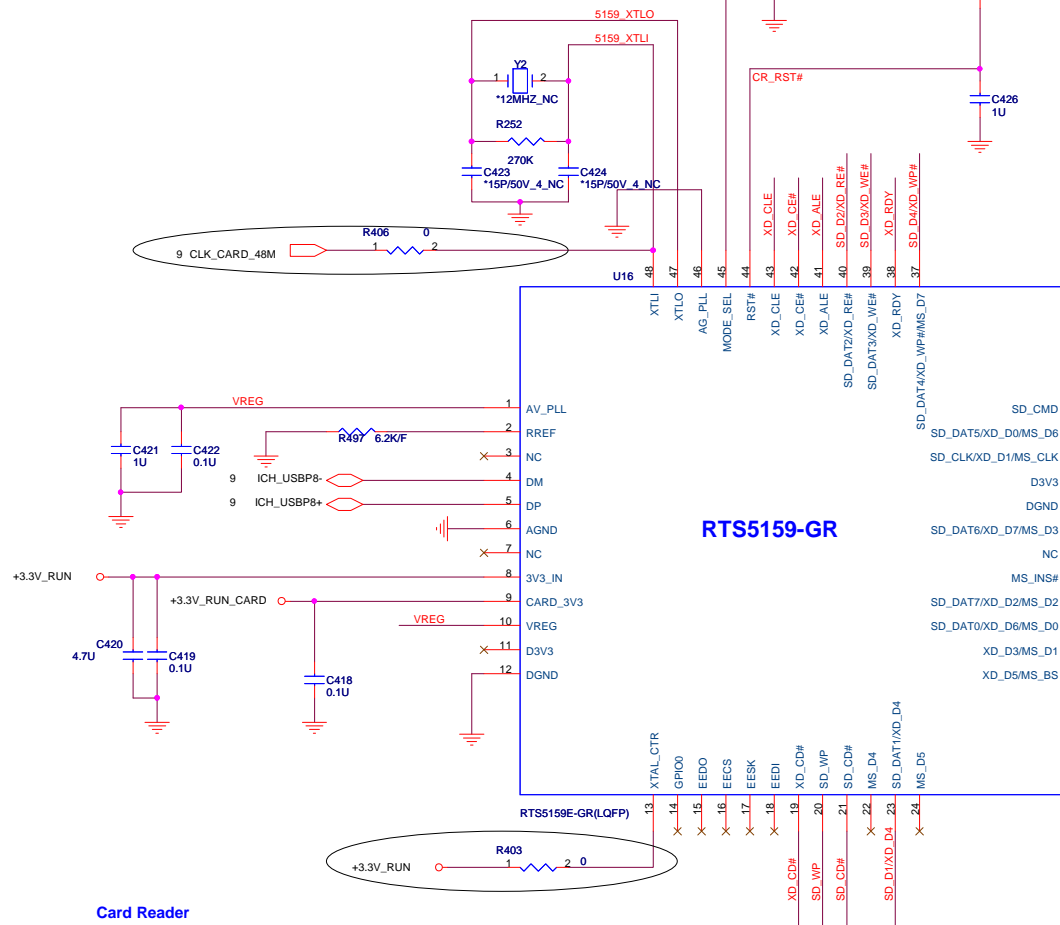
Remember to keep 1M
connection when
remove dongle circuit.



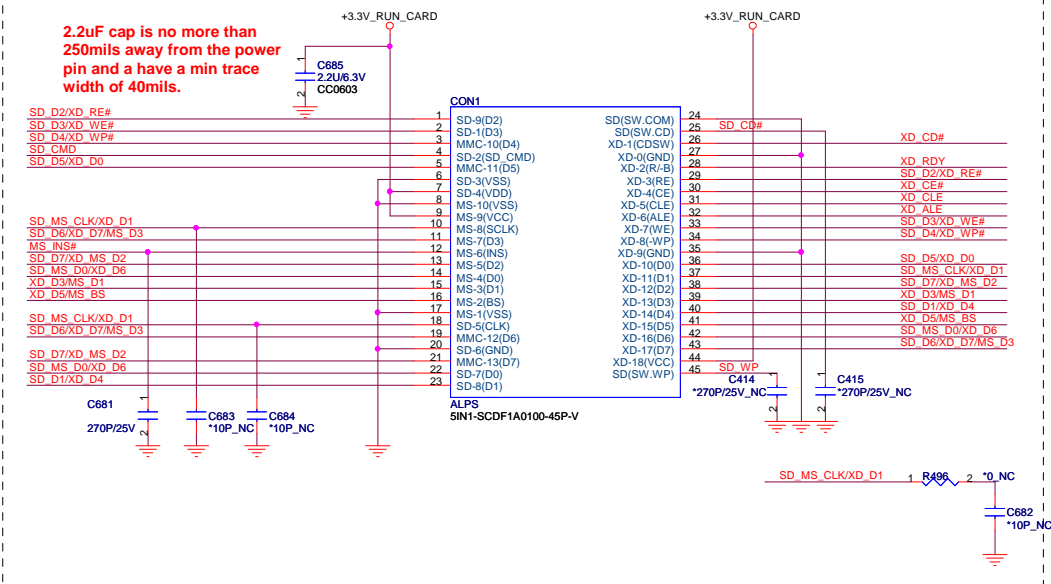
Title			MINI Display Port CONN
Size	Document Number	Rev 1A	
Date:	Thursday, October 08, 2009	Sheet	25 of 62

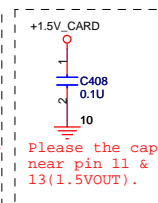


1007 Steg : Reserve 48Mhz for Card Reader for Cost Down

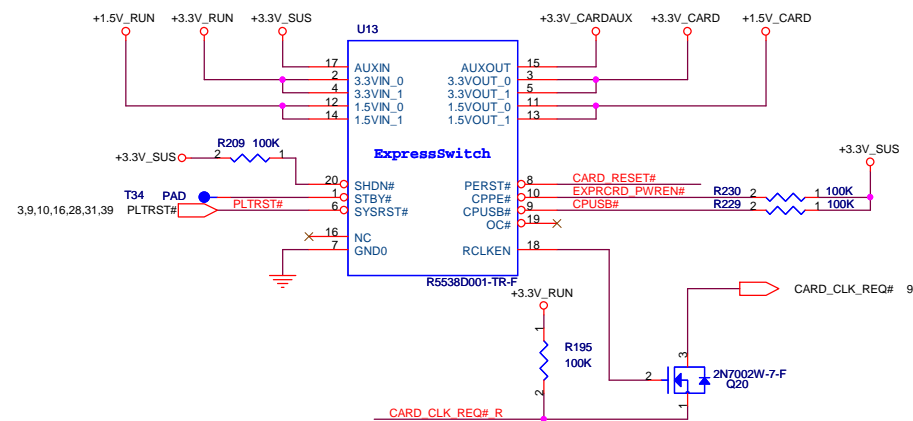


1007 Steg : If 48Mhz must pull high. If 12Mhz must NC.

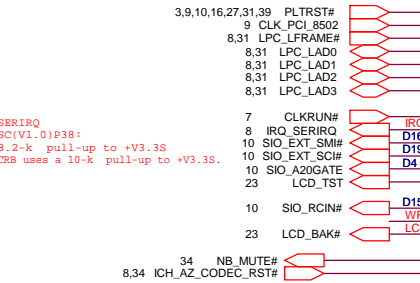
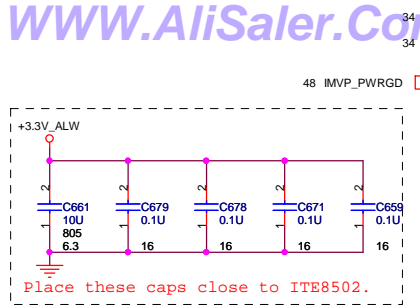




+1.5V_CARD Max. 650mA, Average 500mA.
+3V_CARD Max. 1300mA, Average 1000mA.



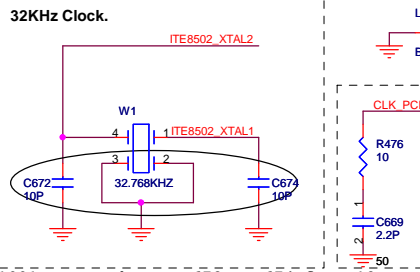
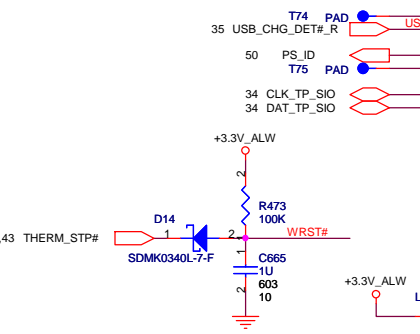
PCI-Express TX and RX direct to connector.



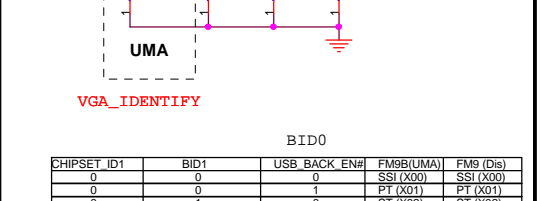
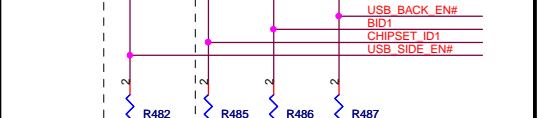
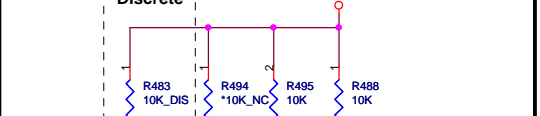
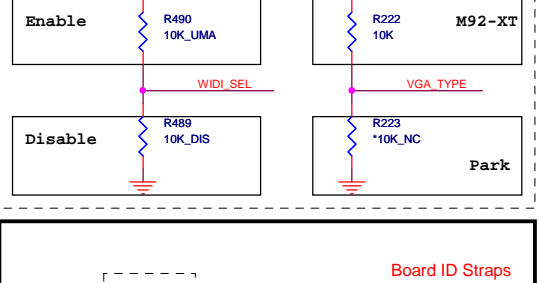
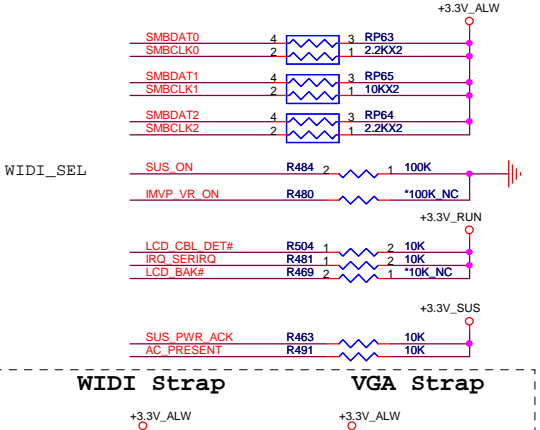
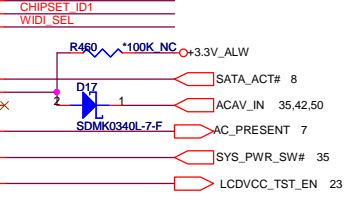
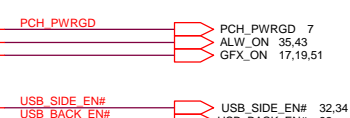
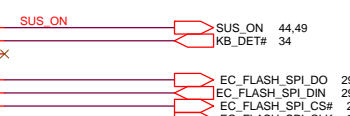
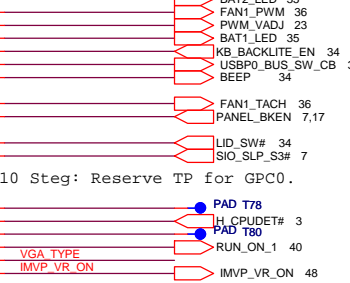
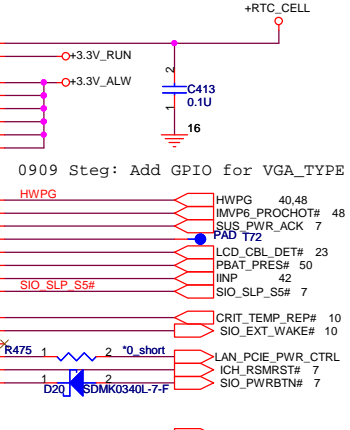
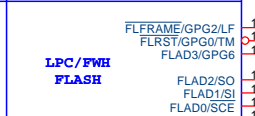
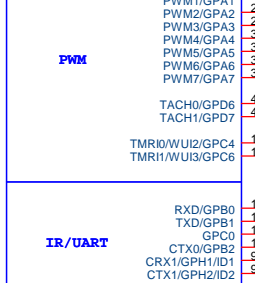
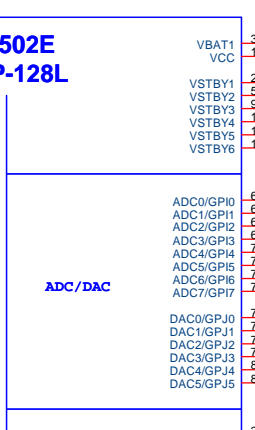
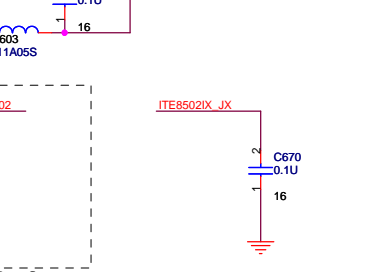
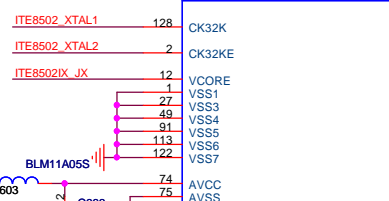
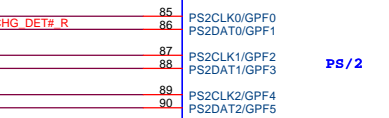
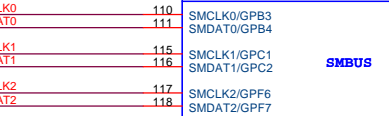
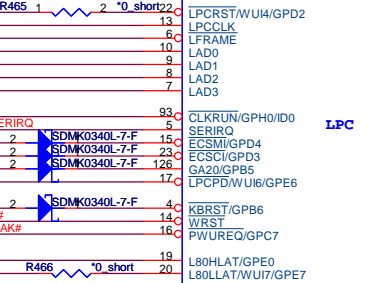
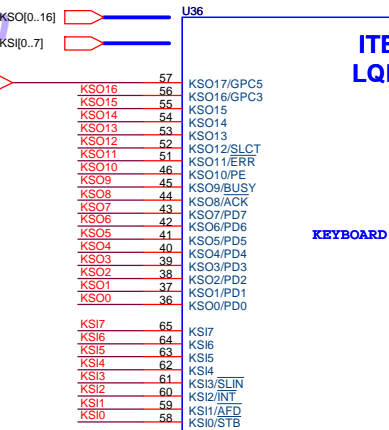
Charge & BAT and Thermal

CLK

G_Thermal



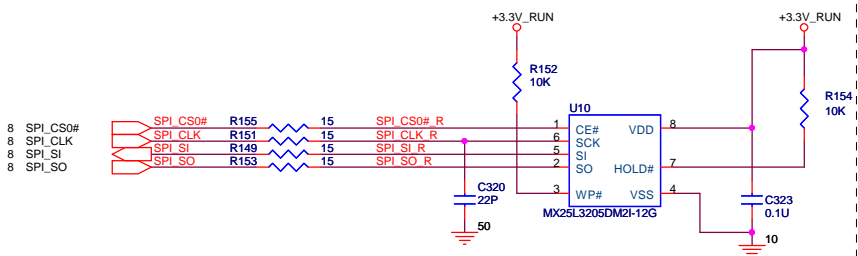
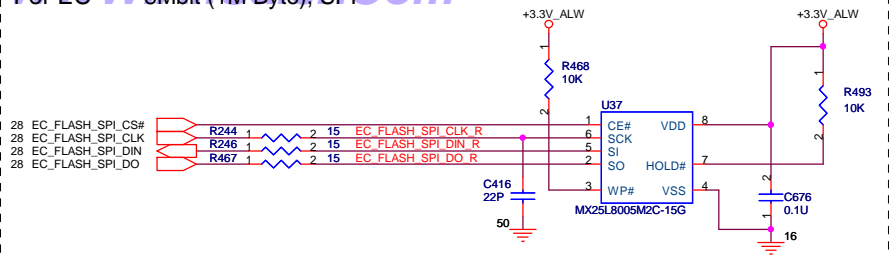
1001 Step: Change C672 & C674 from 18p to 10p for power on sequence.



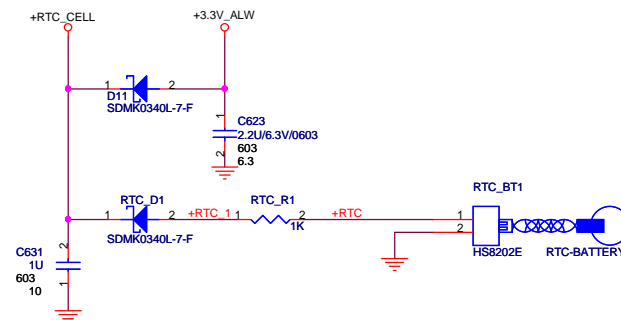
Board ID Straps					
UMA					
VGA_IDENTIFY					
BID0					
CHIPSET_ID1	BID1	USB_BACK_EN#	FMSB(UMA)	FMSB(DIS)	
0	0	0	SS(X00)	SS(X00)	
0	0	1	PT(X01)	PT(X01)	
0	1	0	ST(X02)	ST(X02)	
0	1	1	QT(A00)	QT(A00)	
1	0	0	(A01)	(A01)	
1	0	1			

1001 Step: Change C672 & C674 from 18p to 10p for power on sequence.


For PCH 64Mbit (8M Byte), SPI



RTC BATTERY



```
0818 Steg: Change Location for RTC_D1 & RTC_R1 & RTC_BT1
```

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Title

Briarwood & MINI-PCI CONN

Size

Document Number

RM6

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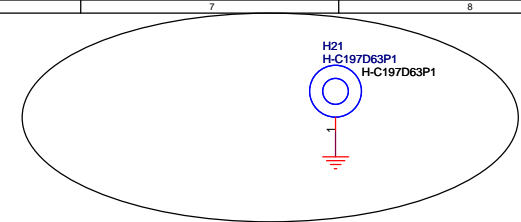
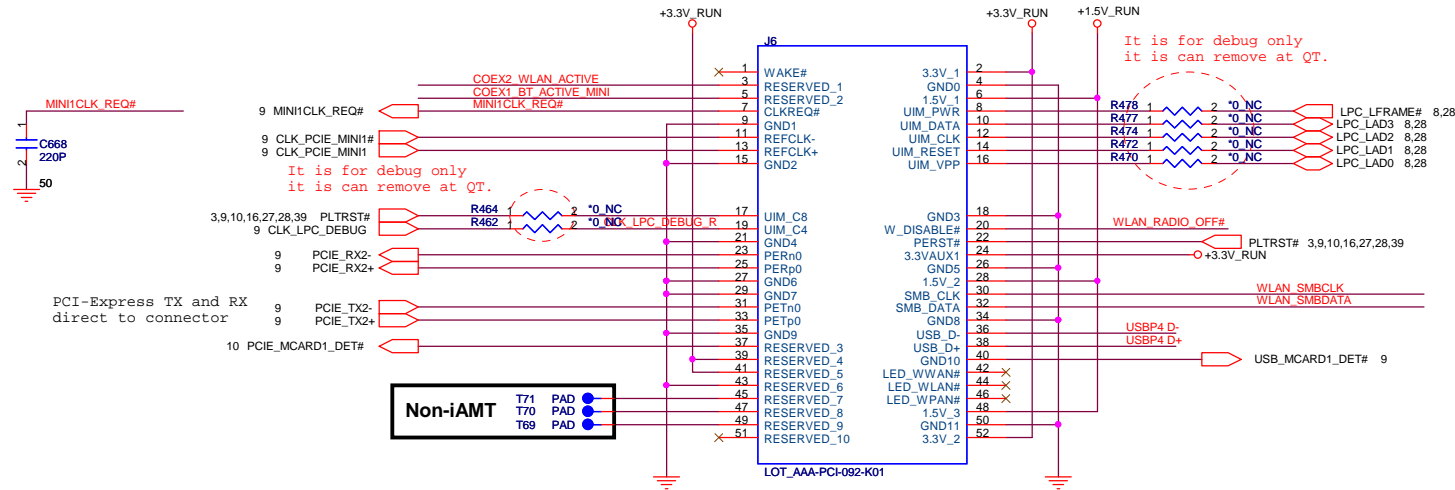
Sheet

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of

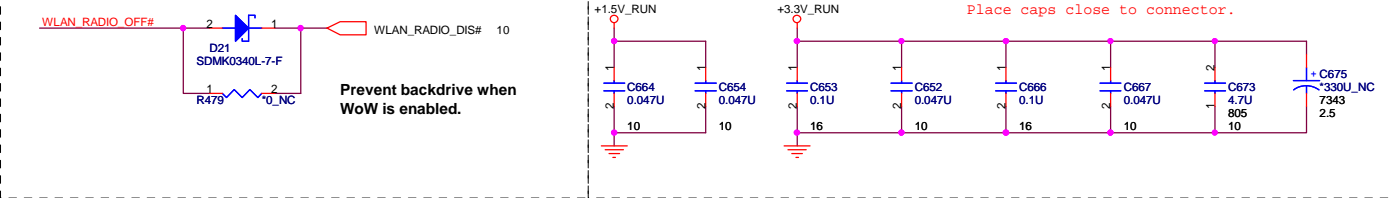
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MiniCard WLAN connector



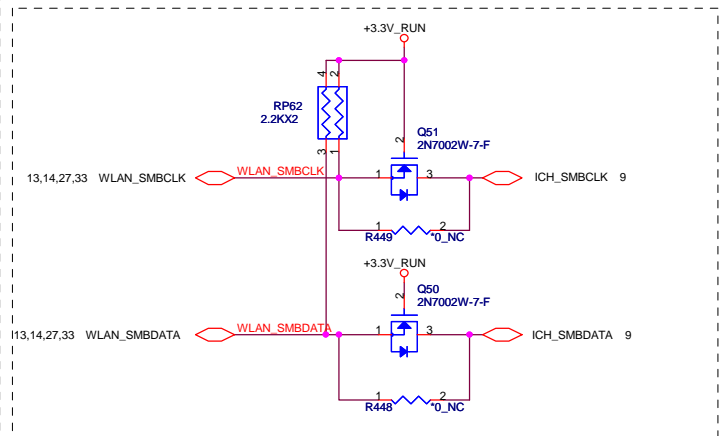
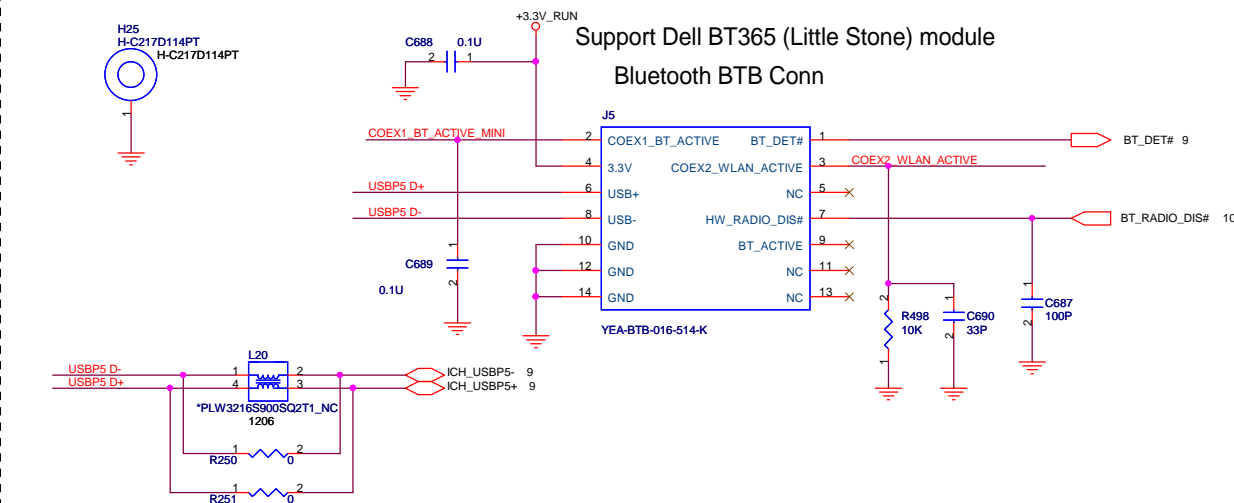
0906 Steg: Remove an Nut H22.

Support for WoW

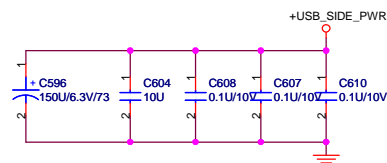
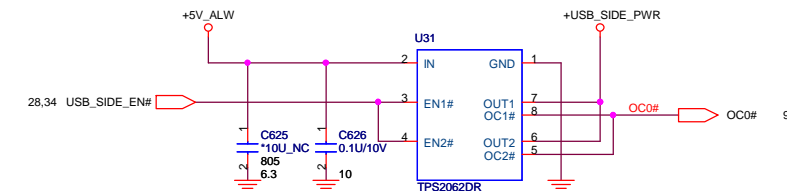


Support Dell BT365 (Little Stone) module

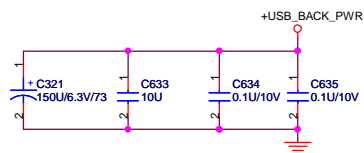
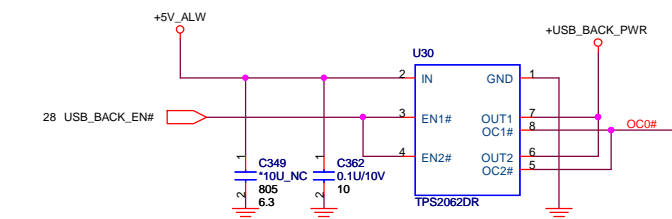
Bluetooth BTB Conn



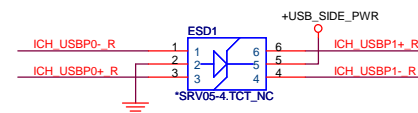
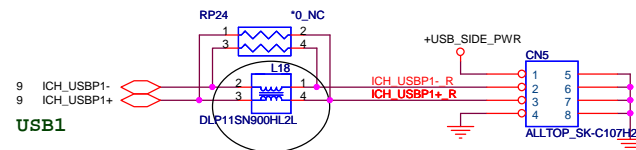
QUANTA COMPUTER		
Title: WLAN & BT CONN		
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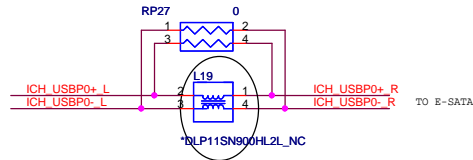
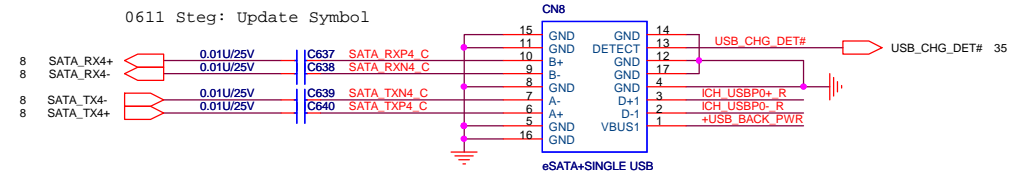
SATA + USB Conn



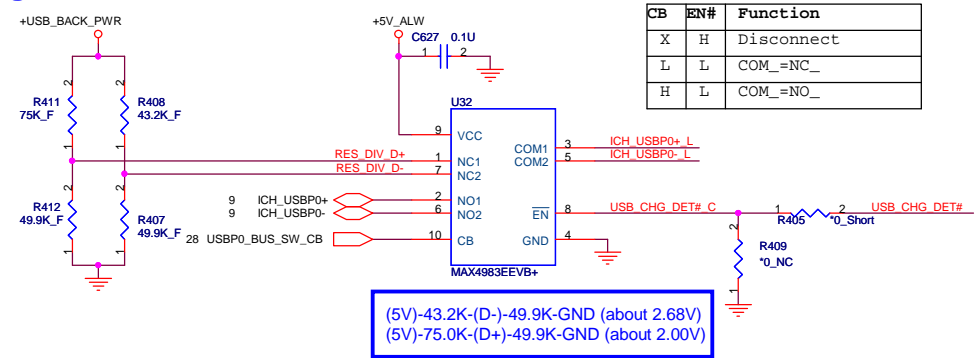
1007 Step : Change L18,L19 Footprint.



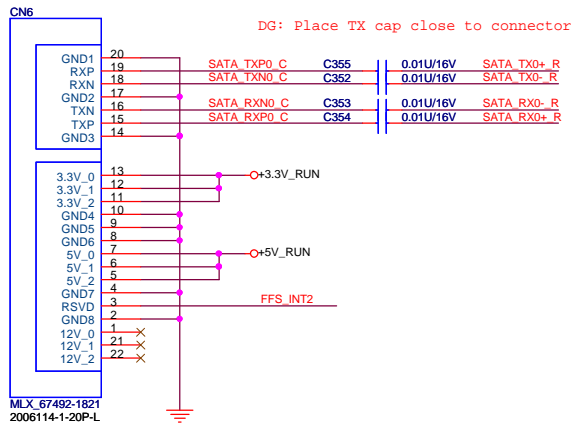
0611 Step: Update Symbol



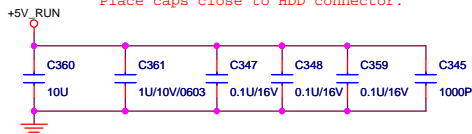
USB Charge



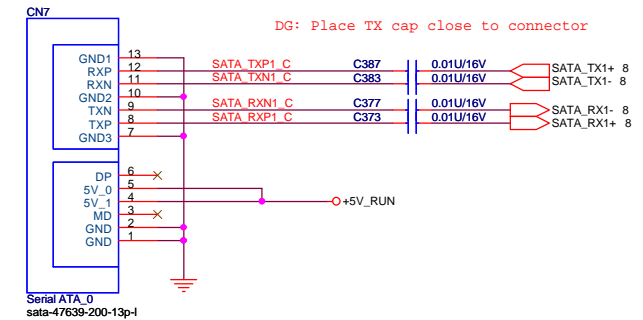
SATA Connector.



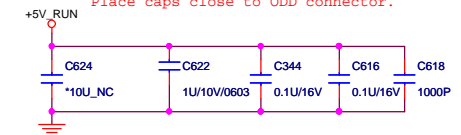
Place caps close to HDD connector.



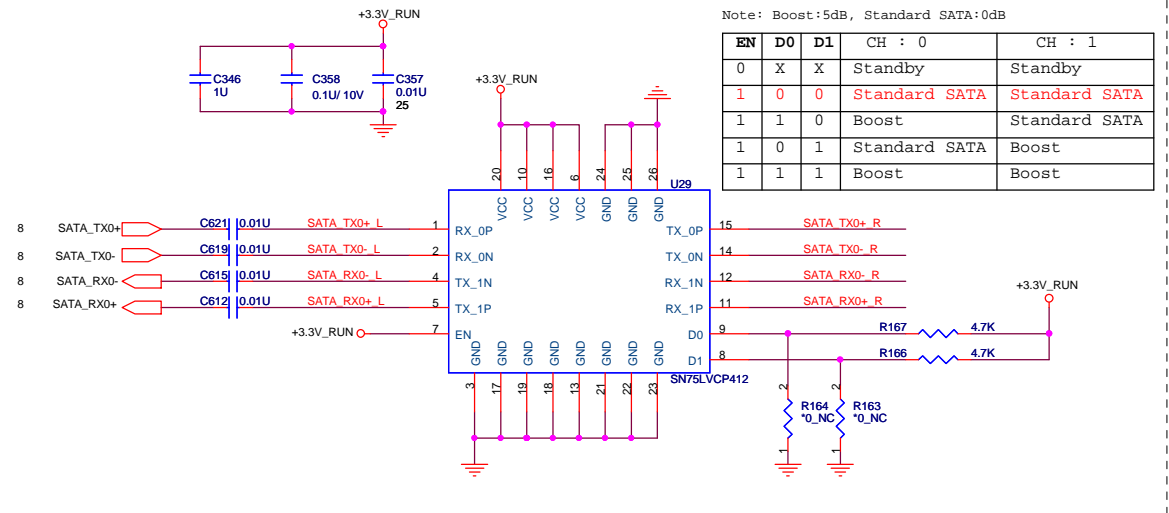
ODD Connector



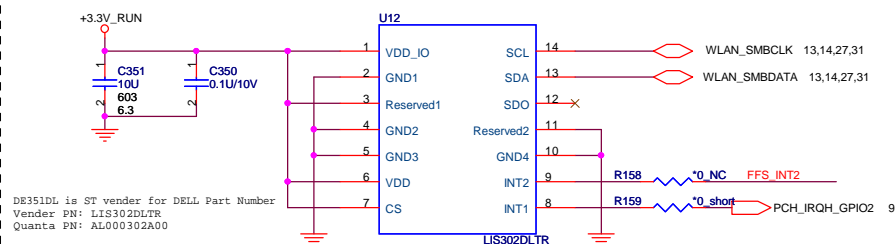
Place caps close to ODD connector.



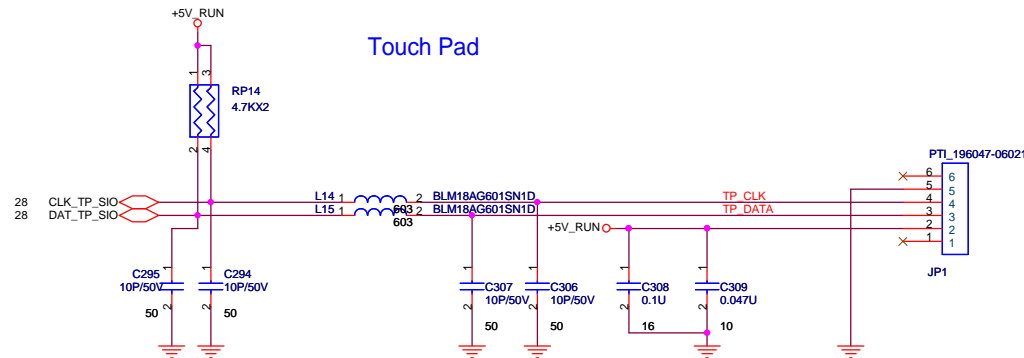
HDD-SATA Re-driver



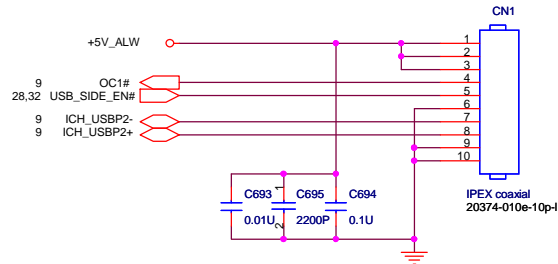
3-axis Fall Sensor (HDD data protector)



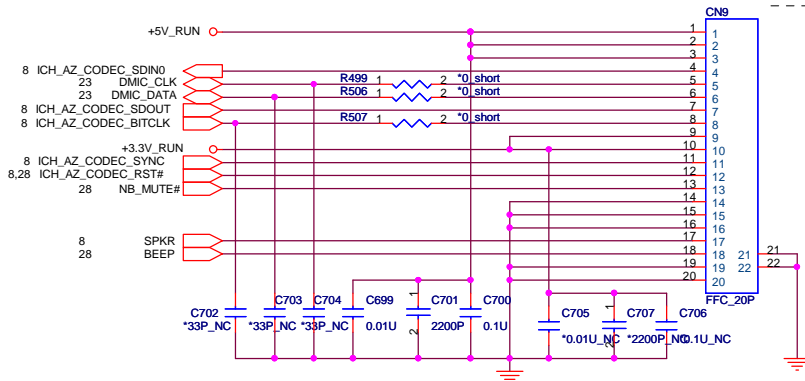
Touch Pad



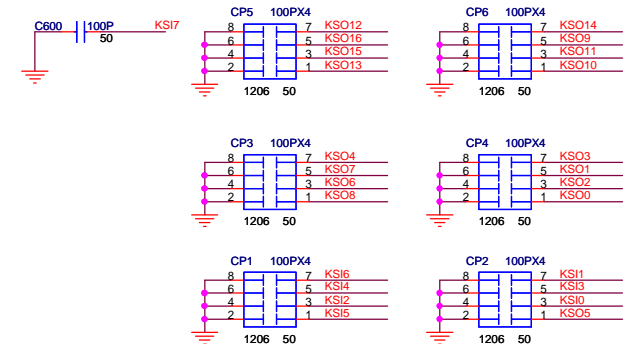
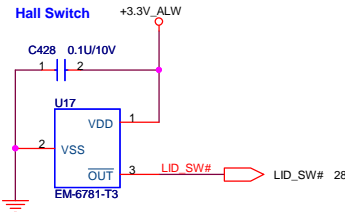
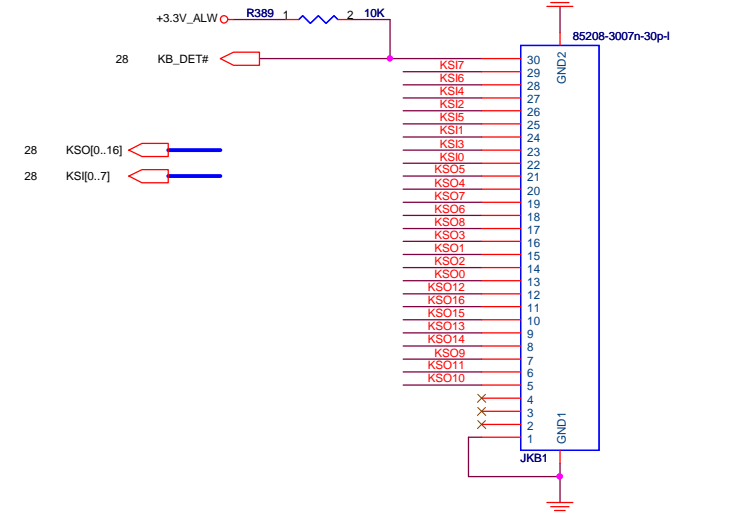
Daughter Board Connector (One USB Port)



Daughter Board Connector (HP & MIC Jack)



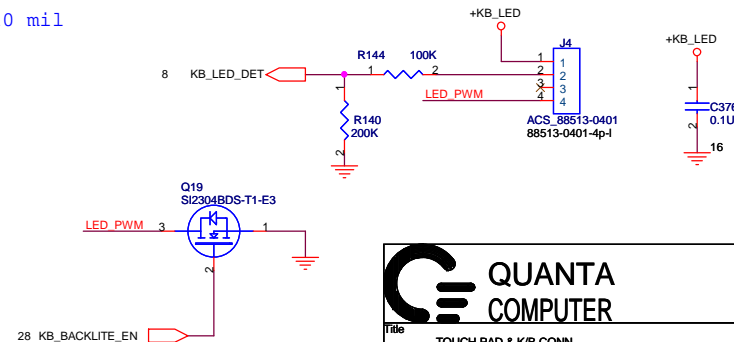
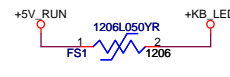
KEYBOARD CONNECTOR



100P CAPS CLOSE TO JKB1

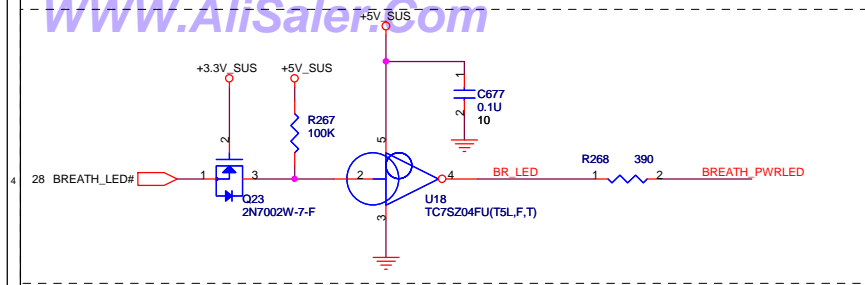
Key board illumination

+KB_LED power trace width >10 mil

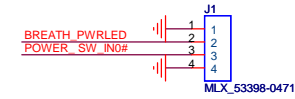


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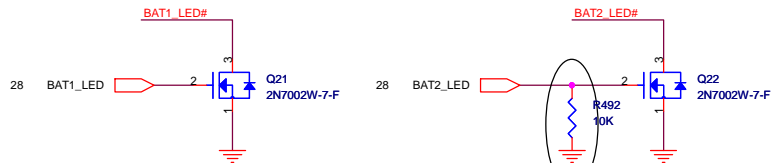
Title TOUCH PAD & K/B CONN		
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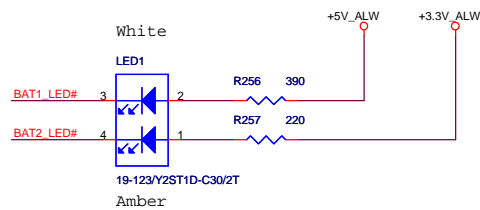
Power button Cable



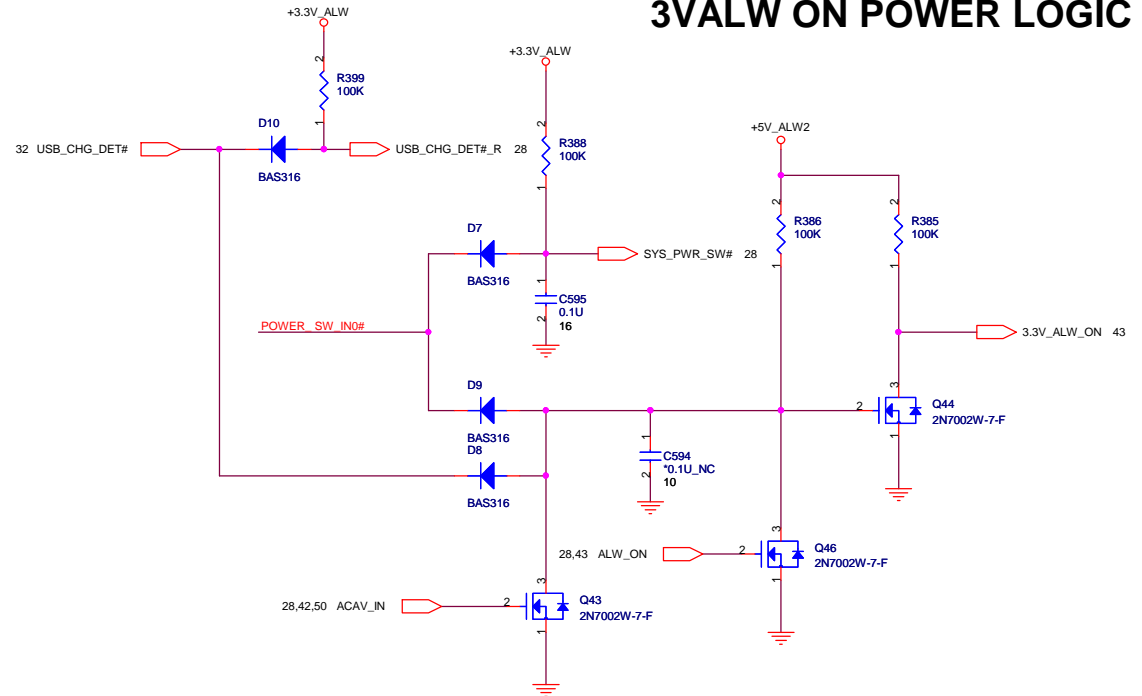
Battery status.



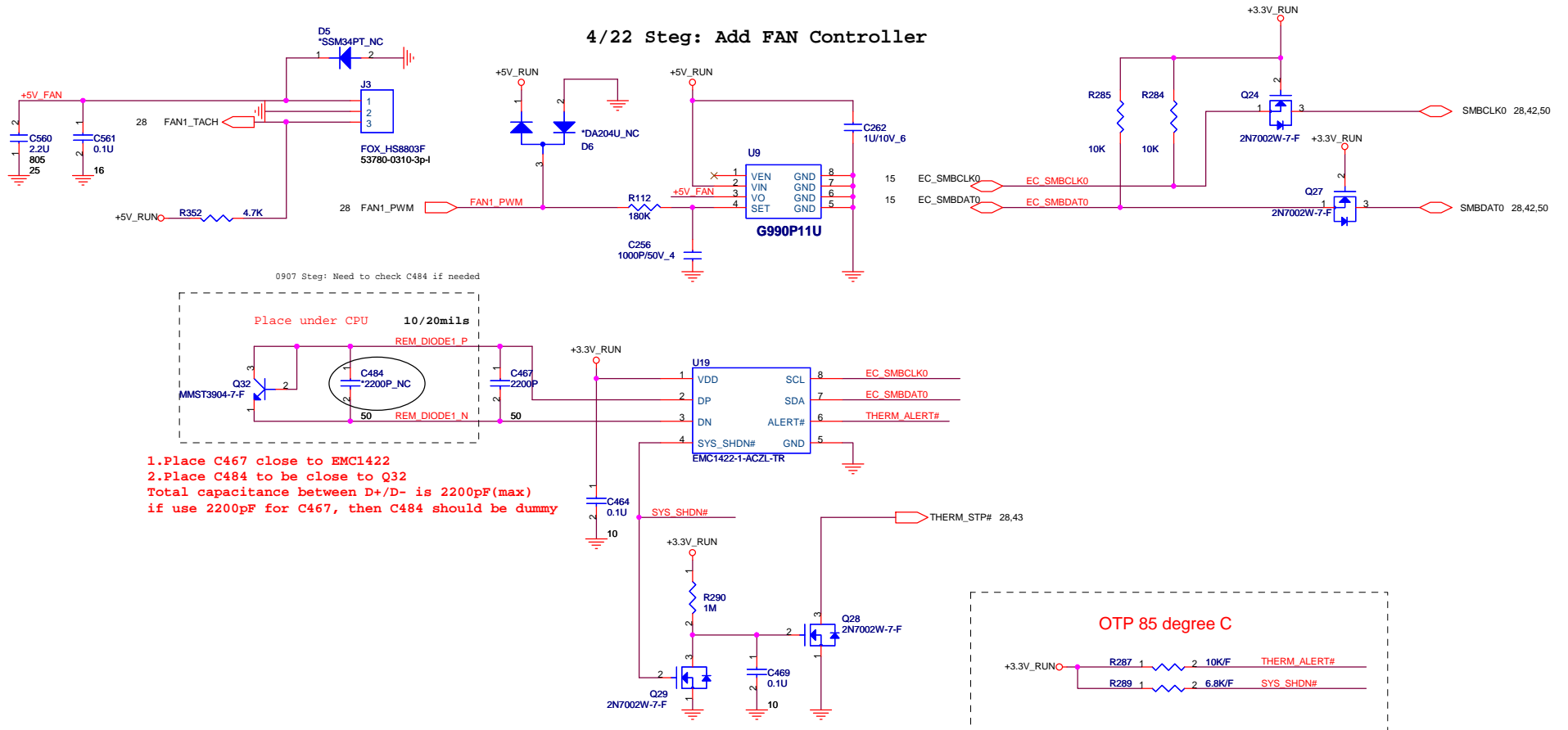
1007 Step : Add an External Pull Down for BAT2_LED




3VALW ON POWER LOGIC



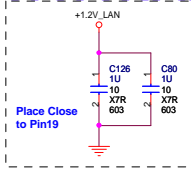
4/22 Steg: Add FAN Controller



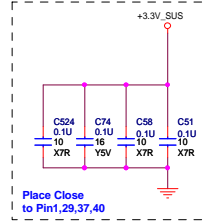
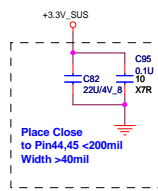
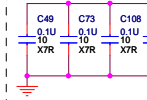
1	2	3	4	5	6	7	8
A							
B							
C							
D							

 **QUANTA
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Title Azella CODEC		
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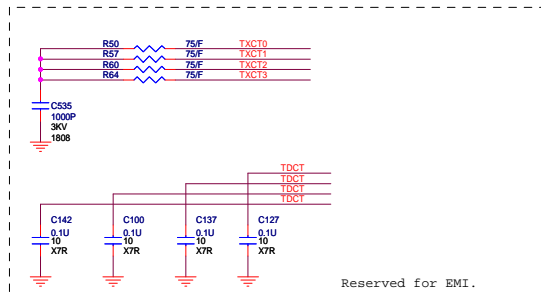
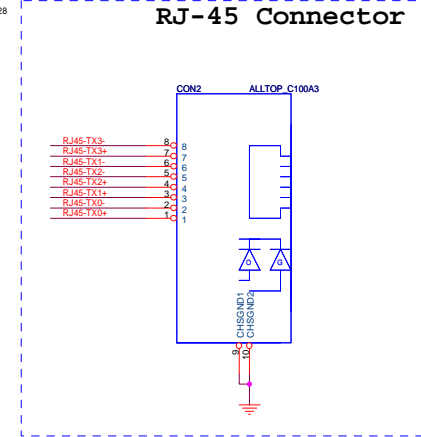
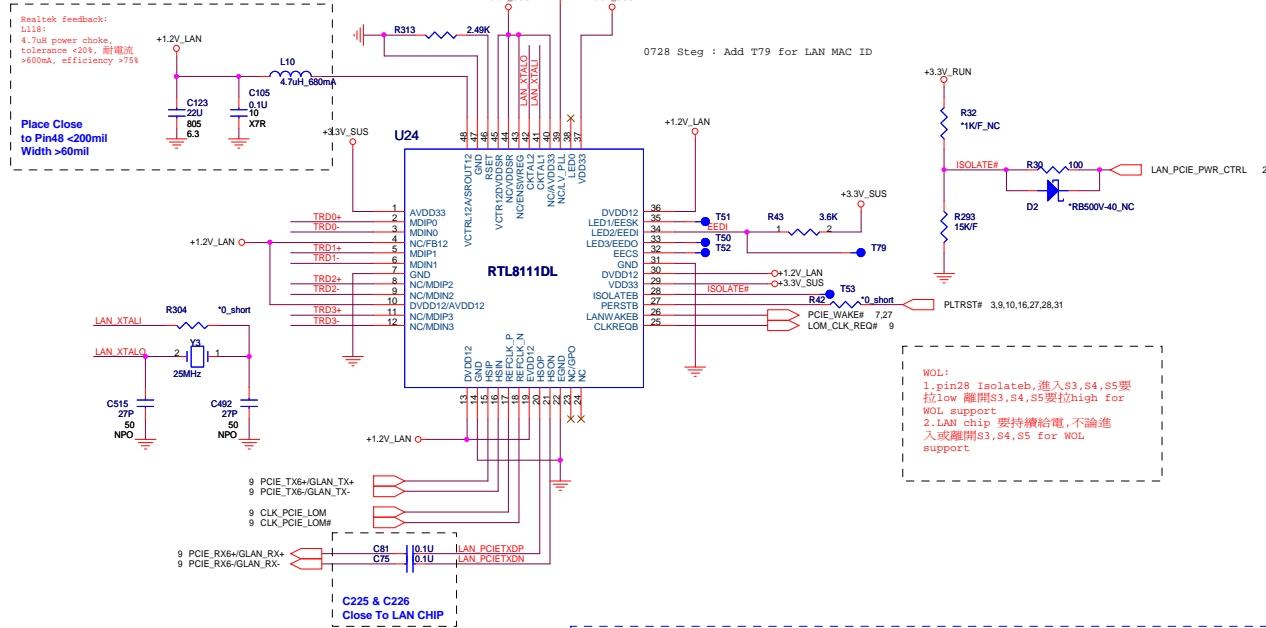


Place Close to Pin10,13,30,36,39

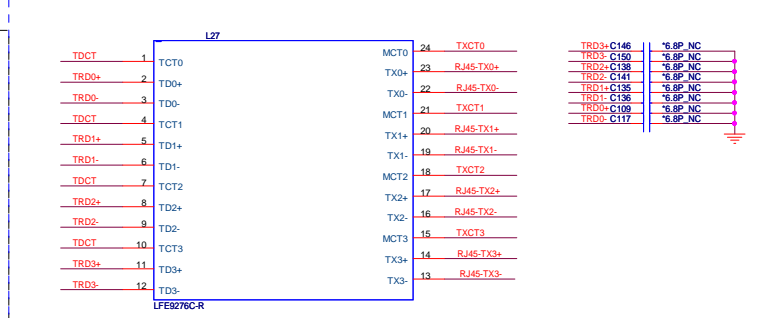


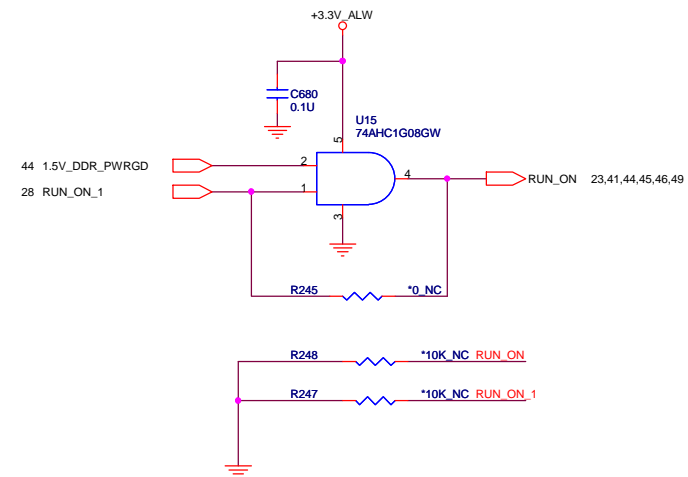
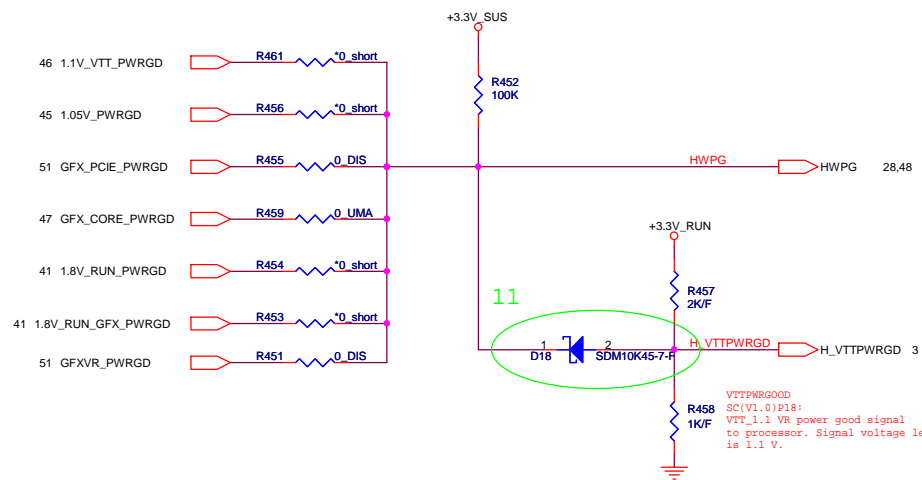
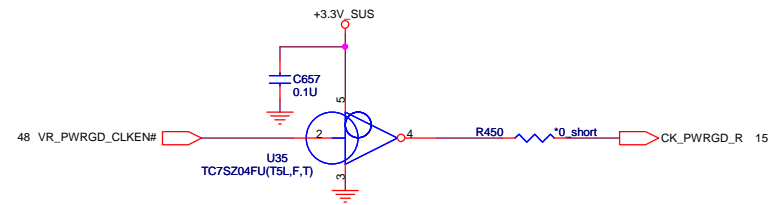
Realtek feedback:
L118:
4.7uH power choke,
tolerance <20%, 耐電流
>600mA, efficiency >75%

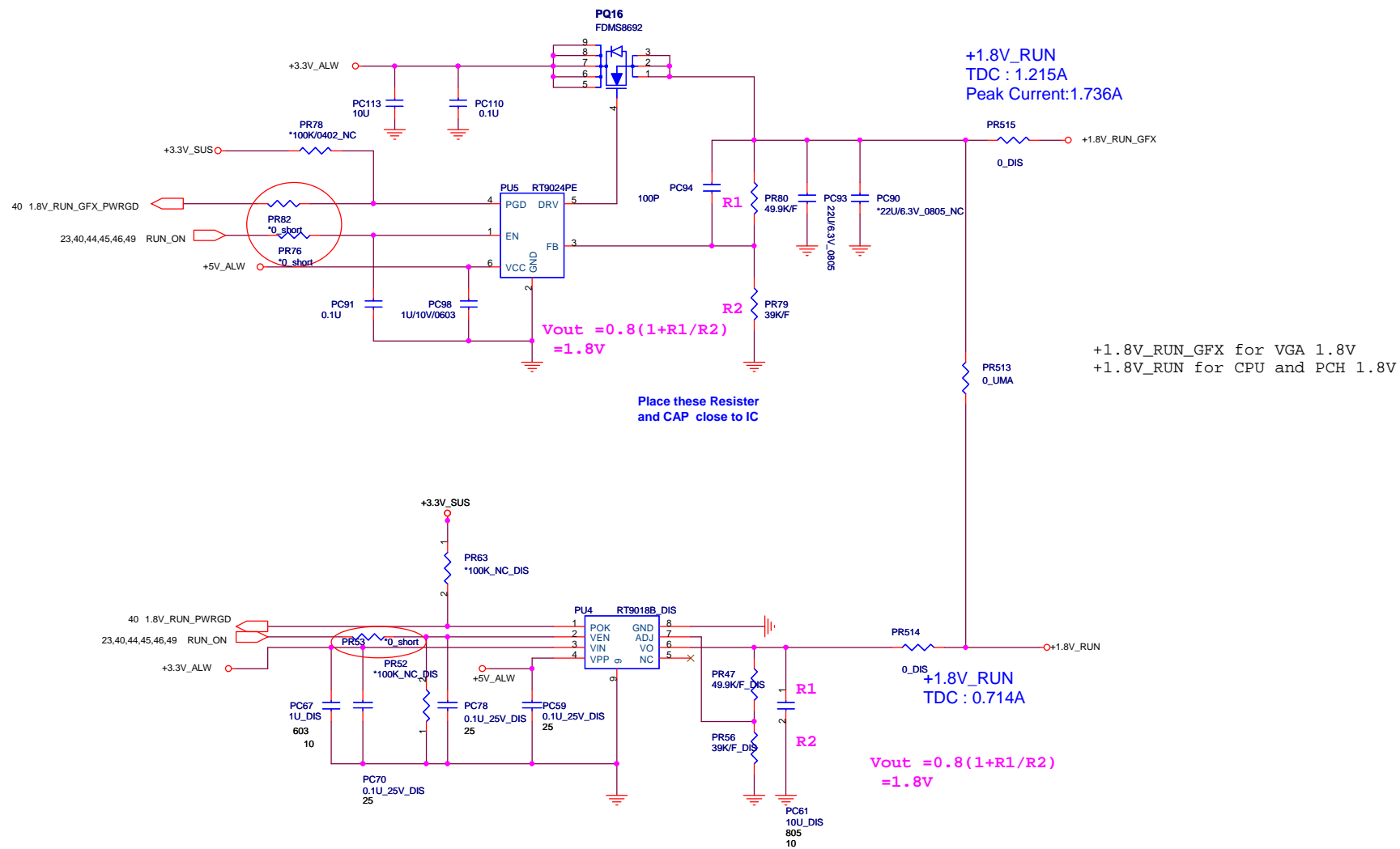
Place Close
to Pin48 <200mil
Width >60mil



LAYOUT NOTE:
CAP CLOSE TO TRANSFORMER
one cap for each pin

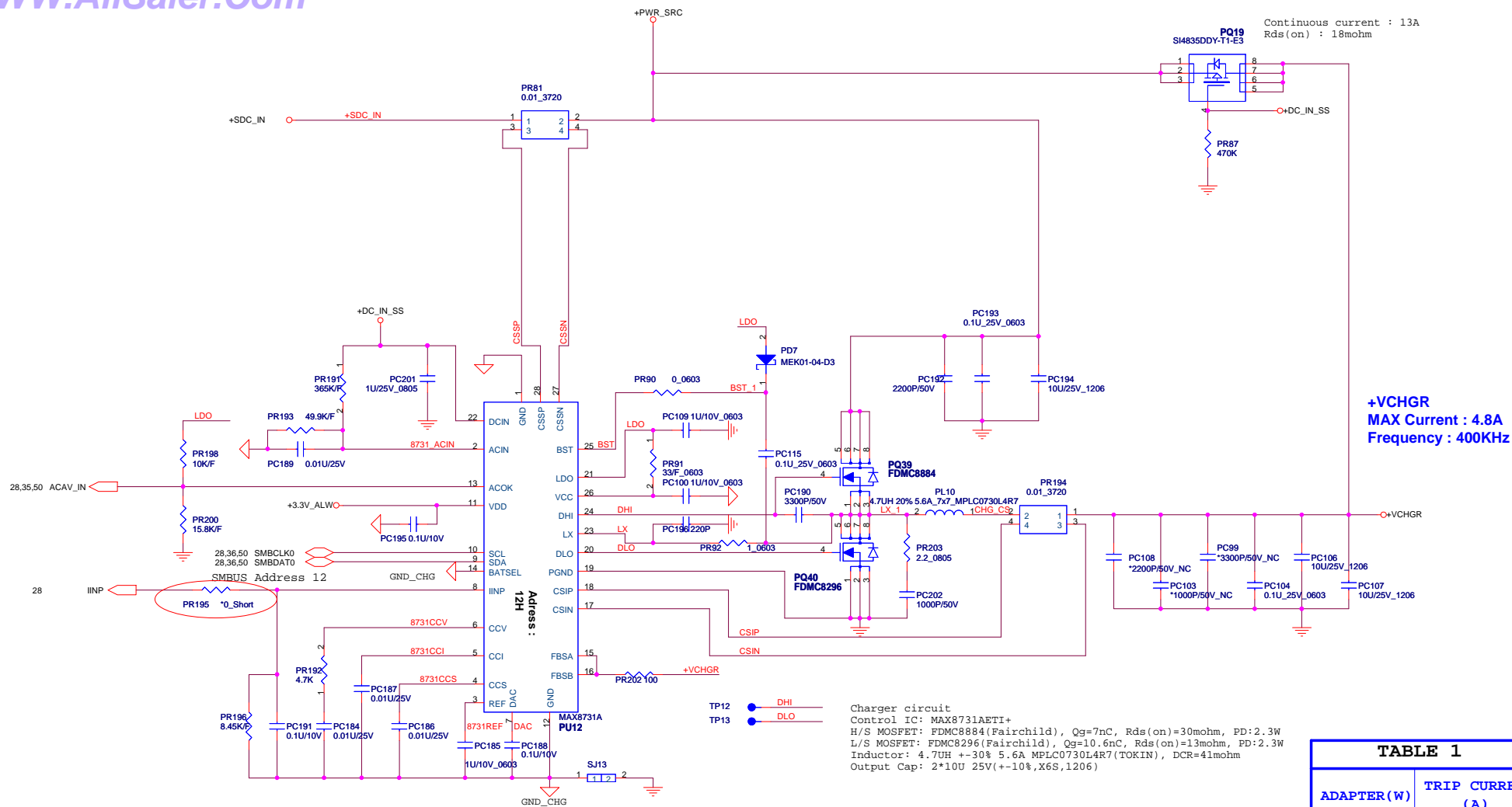






Place these Resistor
and CAP close to IC

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<Title>		
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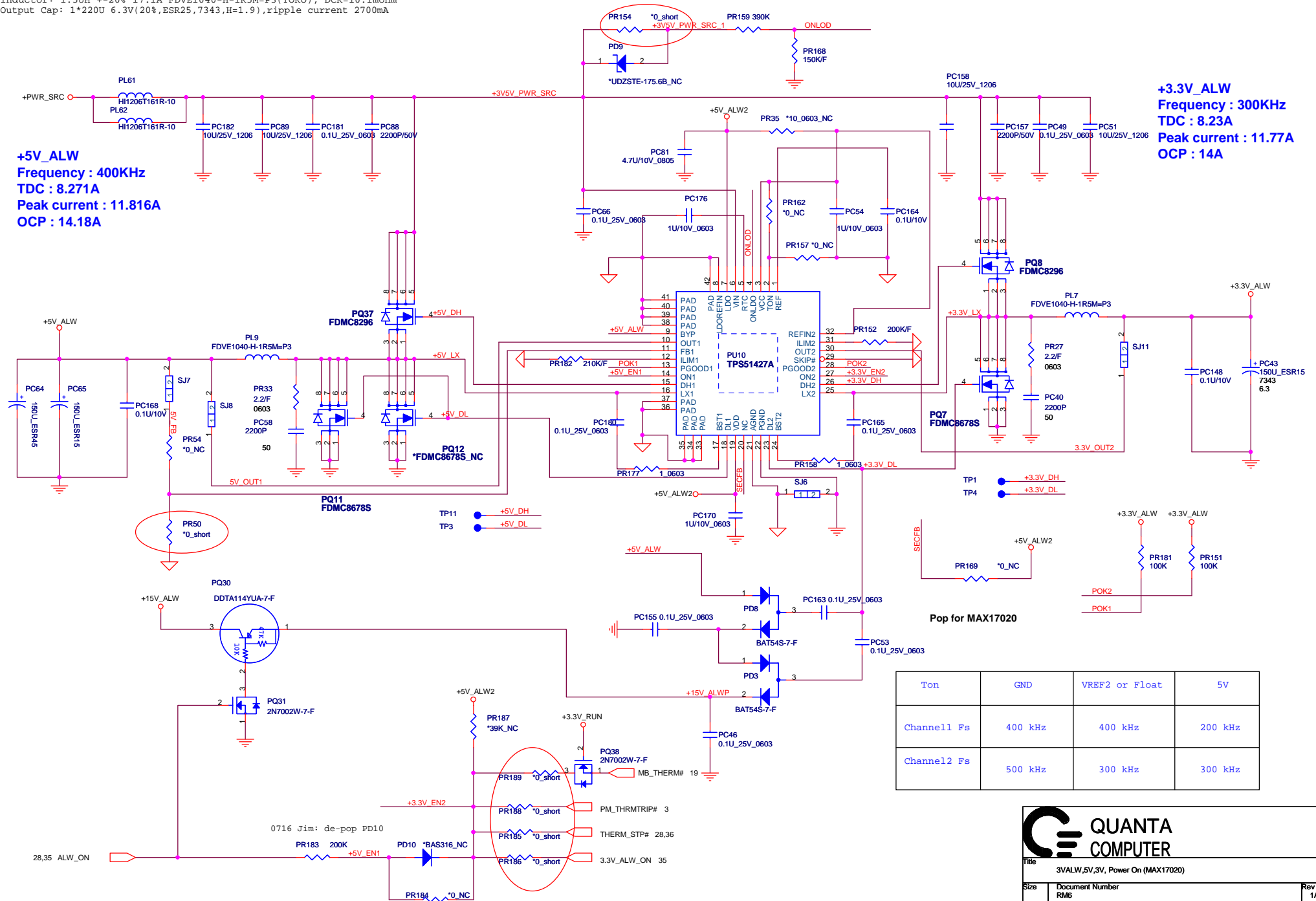


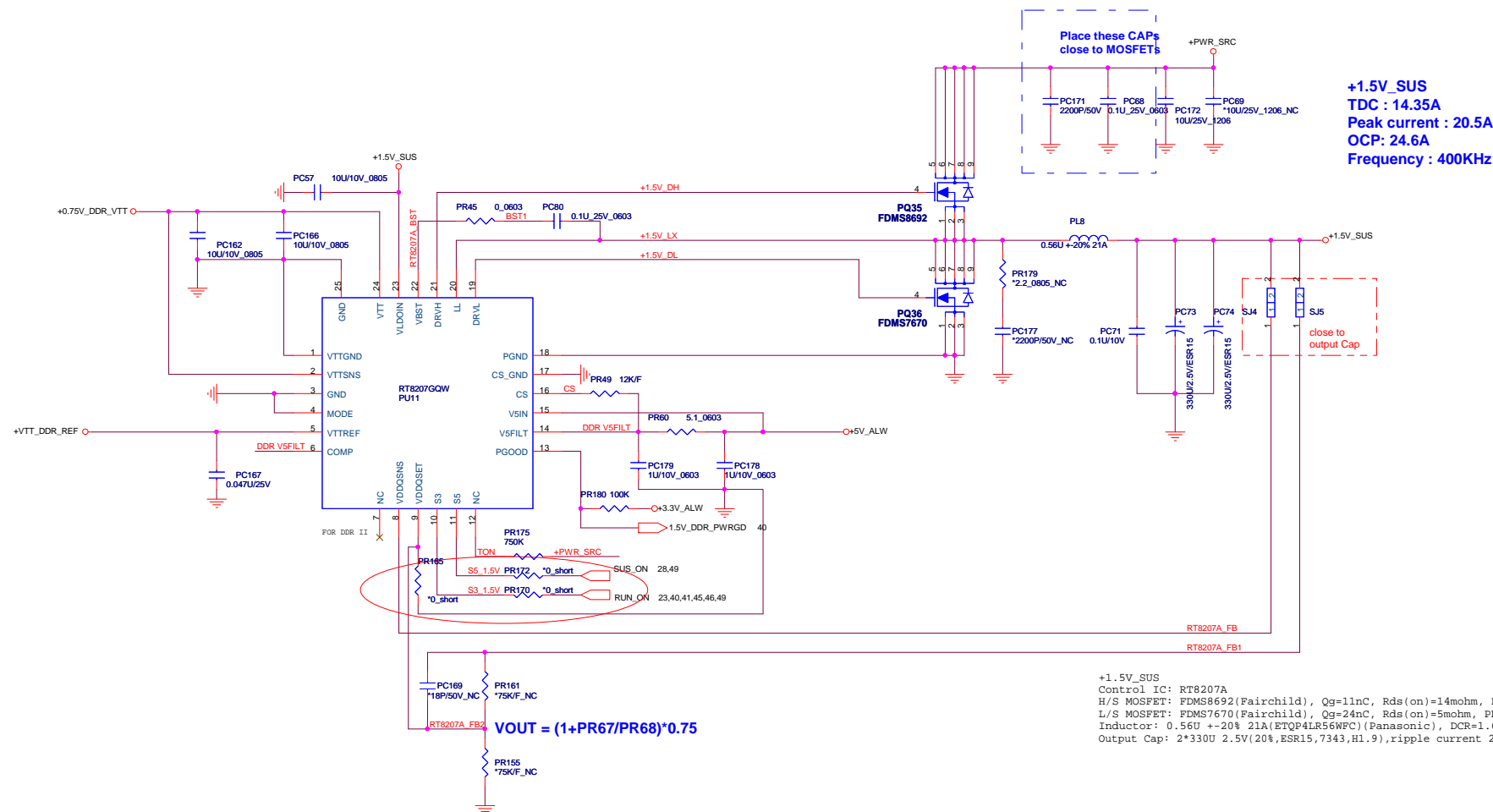
H/S MOSFET: FDMC8296(Fairchild), Qg=10.6nC, Rds(on)=13mohm, PD:2.3W
L/S MOSFET: FDMC8678S(Fairchild), Qg=16nC, Rds(on)=8.7mohm, PD:2.3W
Inductor: 1.5UH +20% 17.1A FDVE1040-H-1R5M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*220U 6.3V(20%,ESR25,7343,H=1.9),ripple current 2700mA

```

+3.3V_ALW
Control IC: TPS51427A
H/S MOSFET: FDMC8296(Fairchild), Qg=10.6nC, Rds(on)=13mohm, PD=2.3W
L/S MOSFET: FDMC8678S(Fairchild), Qg=16nC, Rds(on)=8.7mohm, PD=2.3W
Inductor: 1.5UH +-20% 17.1A FDVE1040-H-1R5M=P3(TOKO), DCR=10.1mohm
Output Cap: 1*150U 6.3V(20%,ESR15,7343,H=1.9),ripple current 2700mA

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VDDQ and VTT discharge control

MODE pin	Discharge mode
V5IN	No discharge
VDDQ	Tracking discharge
S4/GND	Non-tracking discharge

VDDQ output voltage selection

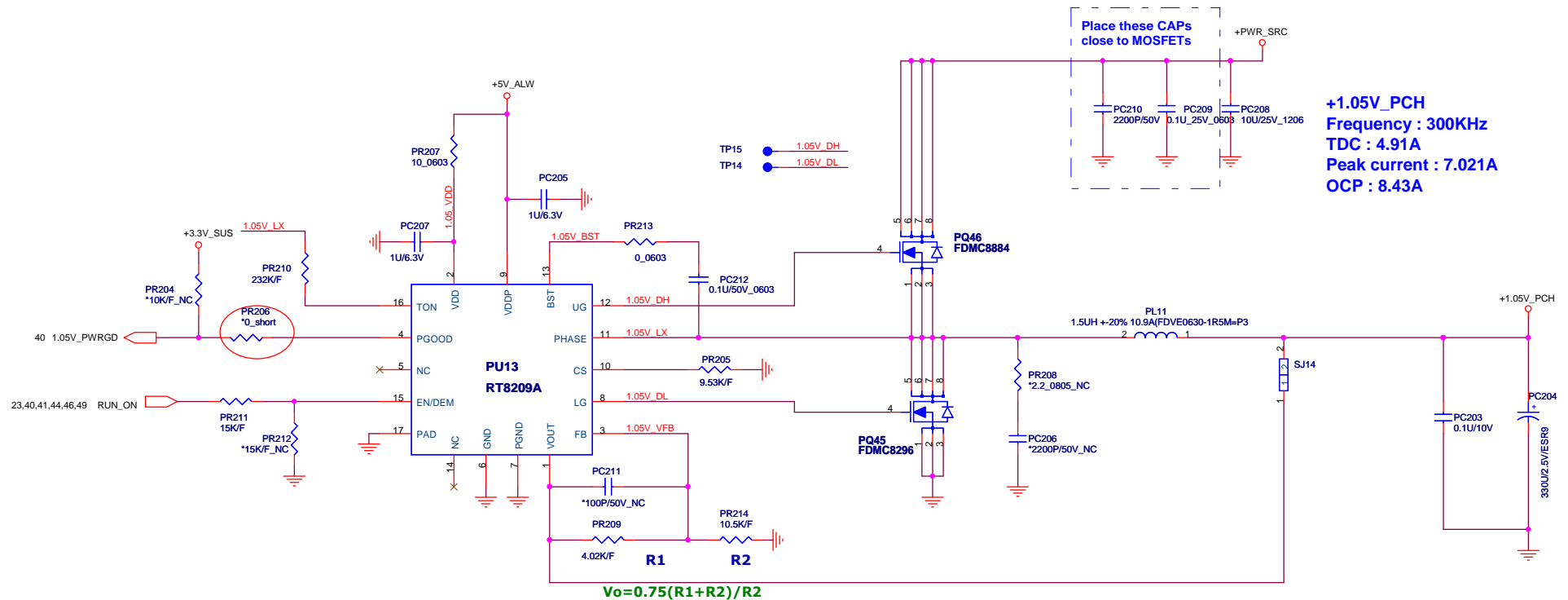
VDDQSET	VDDQ(V)	VTTREF and VTT	NOTE
GND	1.5V	VDDQSNS/2	DDR3
V5IN	1.8V	VDDQSNS/2	DDR2
FB Resistors	Adjusting	VDDQSNS/2	1.5V < VVDDQ < 3V

Outputs Management by S3, S5 control

State	S3	S5	VDDQ	VTTREF	VTT
S0	HI	HI	On	On	On
S3	LO	HI	On	On	Off (Hi-Z)
S4/S5	LO	LO	On (discharge)	Off (discharge)	Off (discharge)

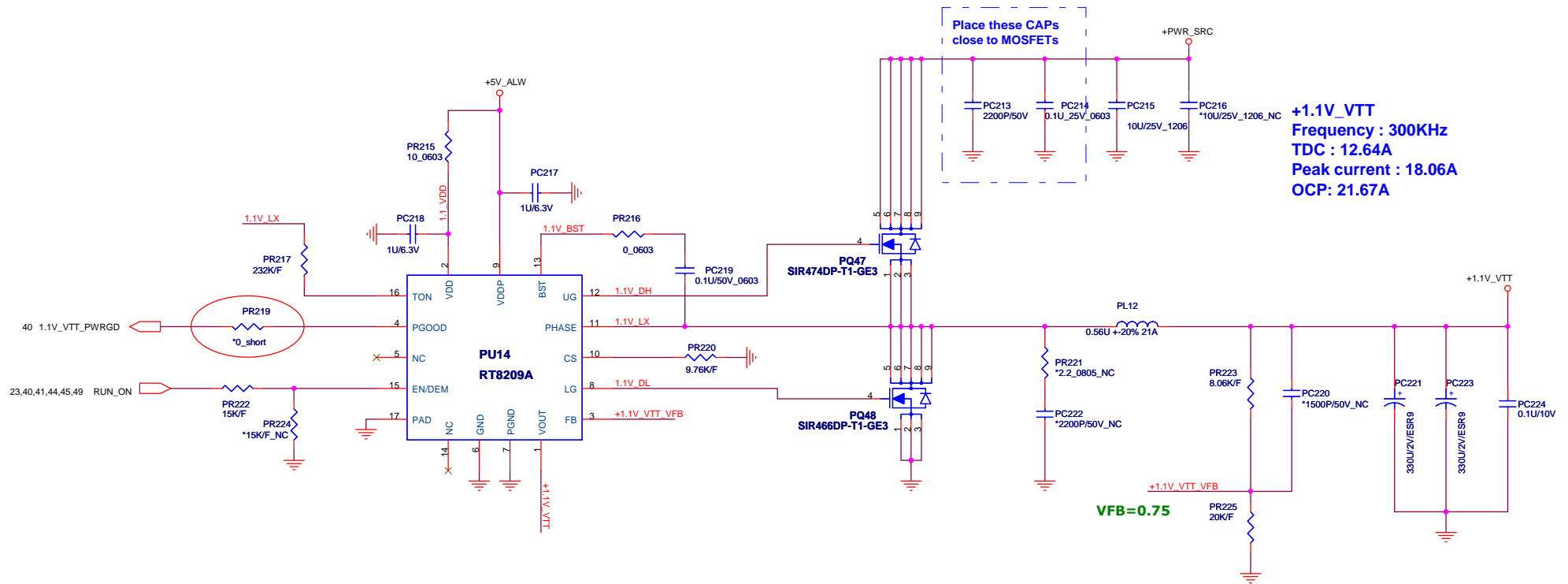


File	1.8VSUS & 0.9VTT (TPS51116)
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+1.05V_PCH
Control IC: RT8209A
H/S MOSFET: FDMC8884(Fairchild), Qg=7nC, Rds(on)=30mohm, PD:2.3W
L/S MOSFET: FDMC8296(Fairchild), Qg=10.6nC, Rds(on)=13mohm, PD:2.3W
Inductor: 1.5UH ±30% 10A SIL104R-1R5B(Delta), DCR=8.1mohm
Output Cap: 1*3300 2.5V(20%,ESR9,7343,H1.9),ripple current 2700mA

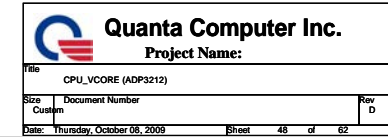
Title			<Title>
Size	Document Number	Rev	
Custom	RMB	1A	
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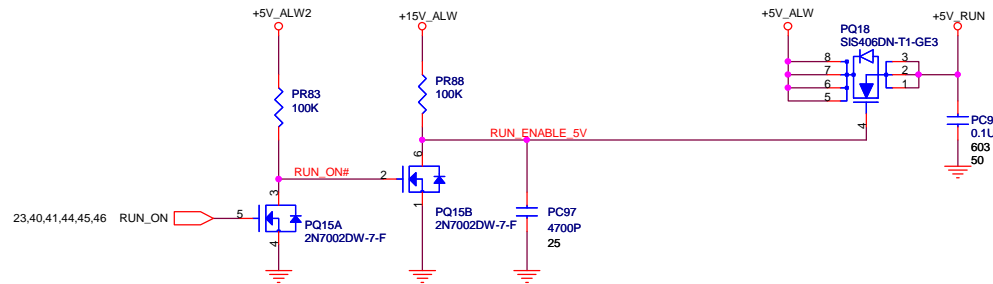
+1.1V_VTT
 Control IC: RT8209A
 H/S MOSFET: SIR474DP(Vishay), Qg=12nC, Rds(on)=12mohm, PD:3.9W
 L/S MOSFET: SIR466DP(Vishay), Qg=33nC, Rds(on)=5.1mohm, PD:5W
 Inductor: 0.56U +-20% 21A(ETQP4LR56WFC)(Panasonic), DCR=1.6mohm
 Output Cap: 2*330U 2V(+10/-35%,7343,ESR=9),ripple current 3000mA

Title		<Title>
Size	Document Number	Rev
Custom	RMB	1A
Date:	Thursday, October 08, 2009	Sheet 46 of 62

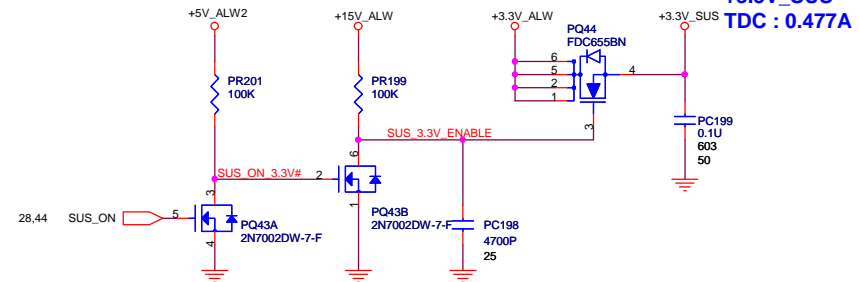




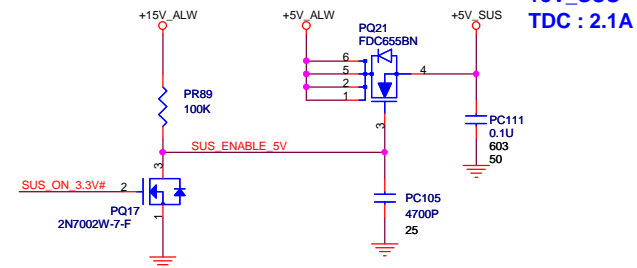
+5V_RUN
TDC : 2.651A



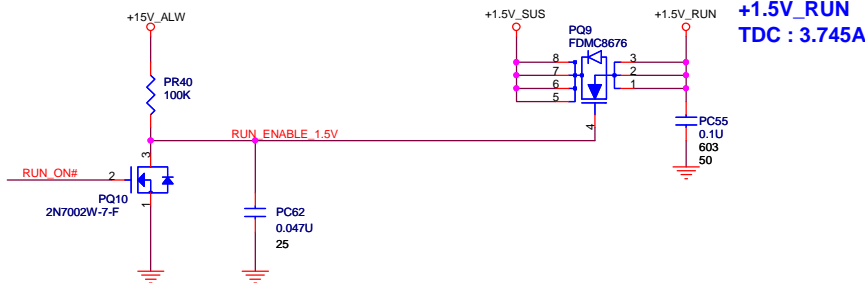
+3.3V_SUS
TDC : 0.477A



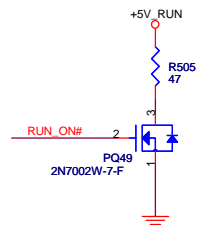
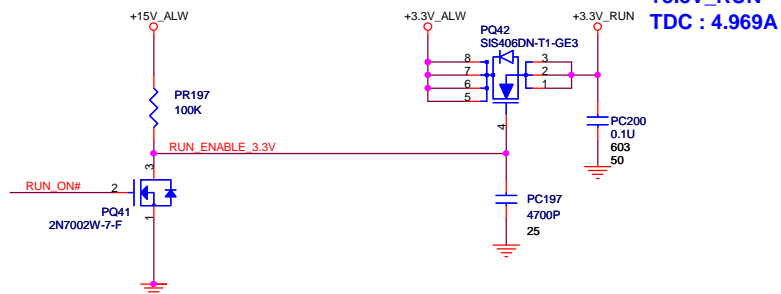
+5V_SUS
TDC : 2.1A




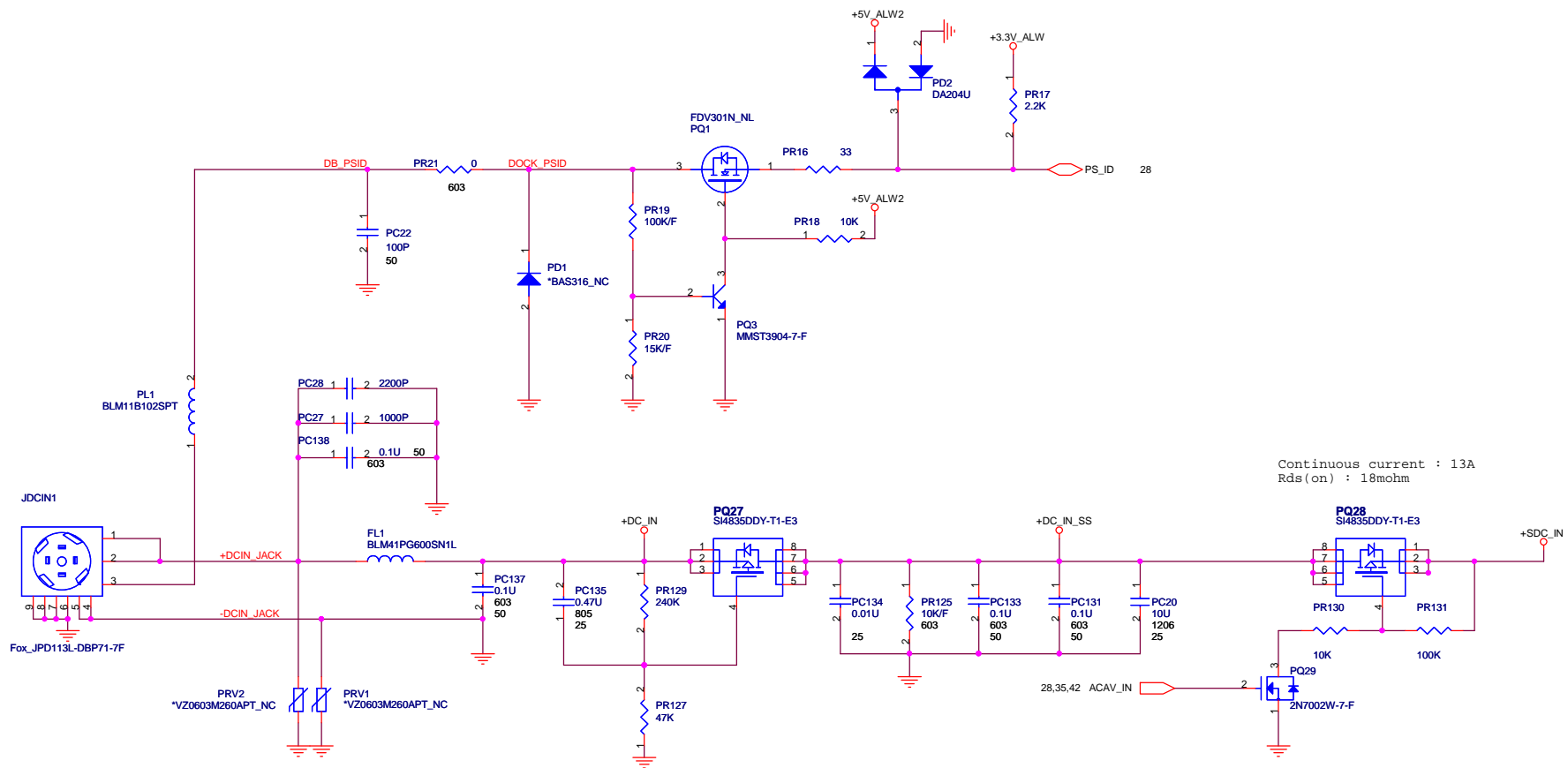
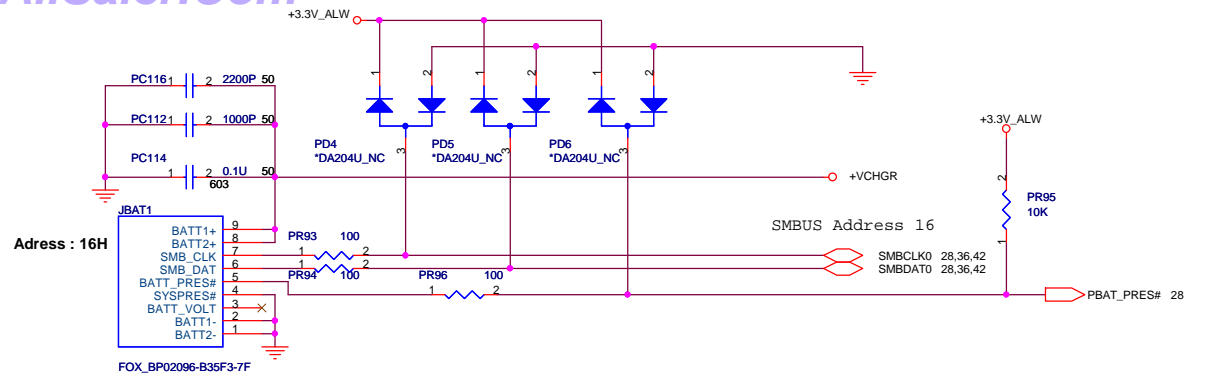
+1.5V_RUN
TDC : 3.745A



+3.3V_RUN
TDC : 4.969A



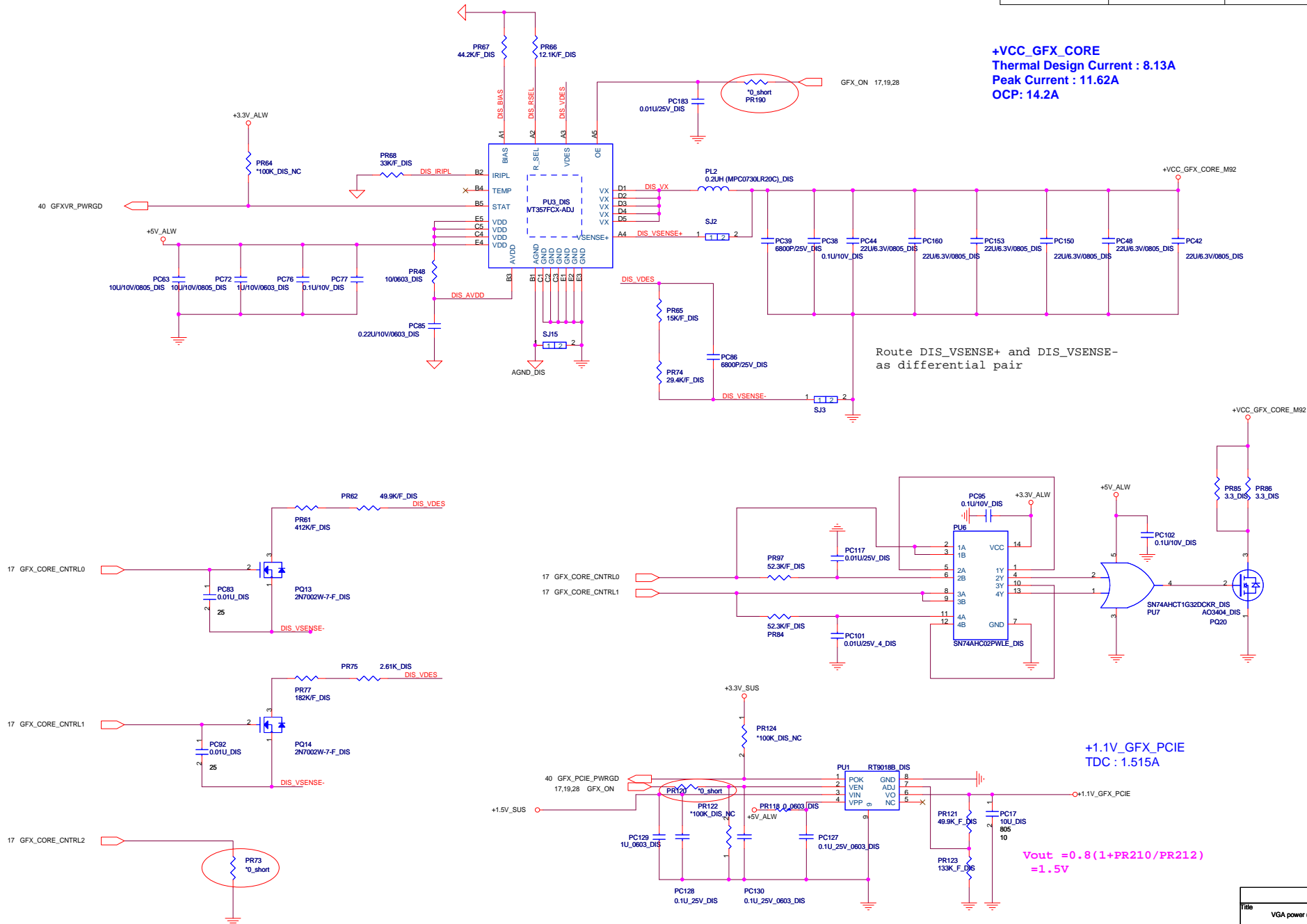
 QUANTA COMPUTER			
Title: RUN POWER SW			
Size: RM6	Document Number		Rev 1A
Date: Thursday, October 08, 2009	Sheet 49	of 62	



+VCC_GFX_CORE_M92

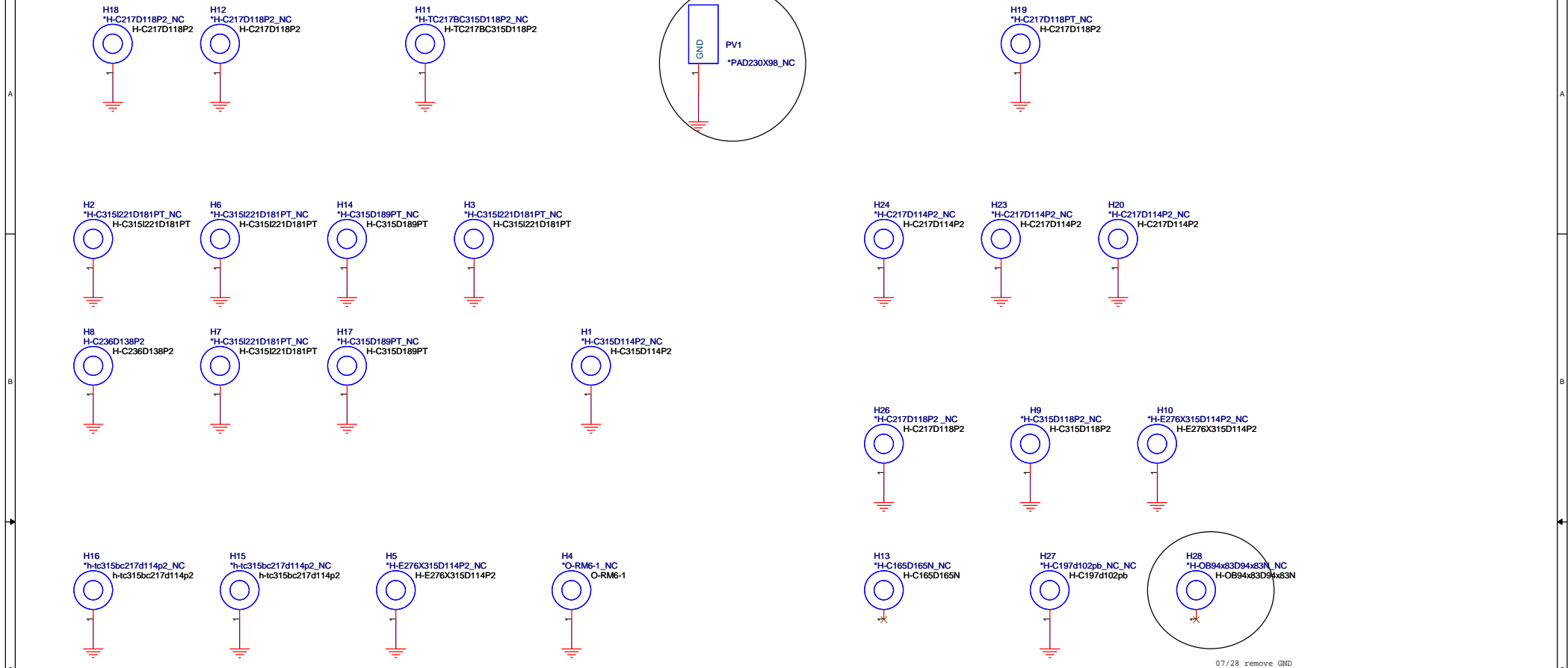
GFX_CORE_CNTRL0	GFX_CORE_CNTRL1	GFX_CORE_CNTRL2	+VCC_GFX_CORE
LOW	LOW	LOW	1.2V
HIGH	LOW	LOW	1.1V
HIGH	HIGH	LOW	0.9V


+VCC_GFX_CORE
Thermal Design Current : 8.13A
Peak Current : 11.62A
OCP: 14.2A




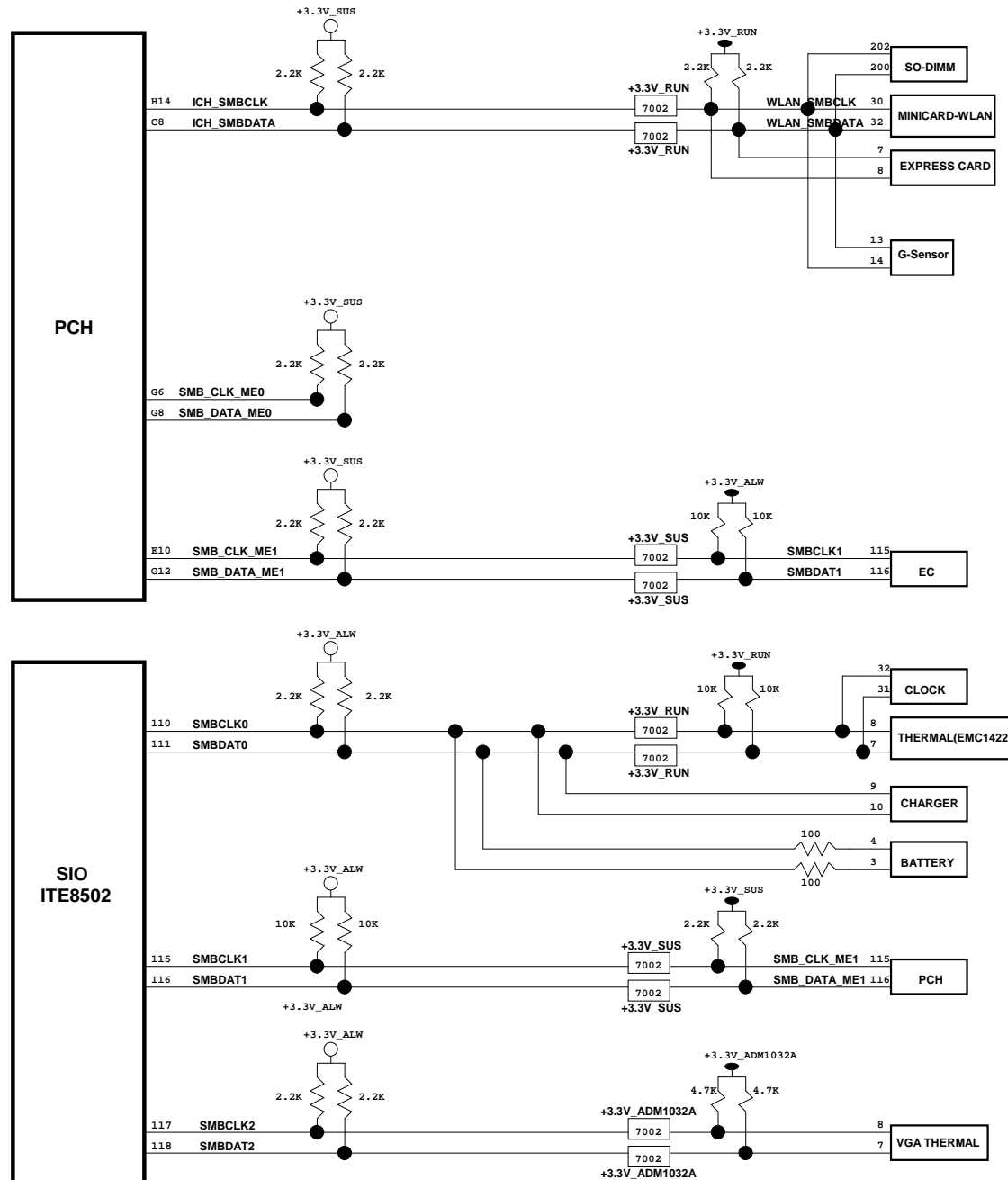
Title		
VGA power (MAX8792 & RT9018B)		
Size	Document Number	Rev
RM6		1A
Date:	Thursday, October 08, 2009	Sheet 51 of 62

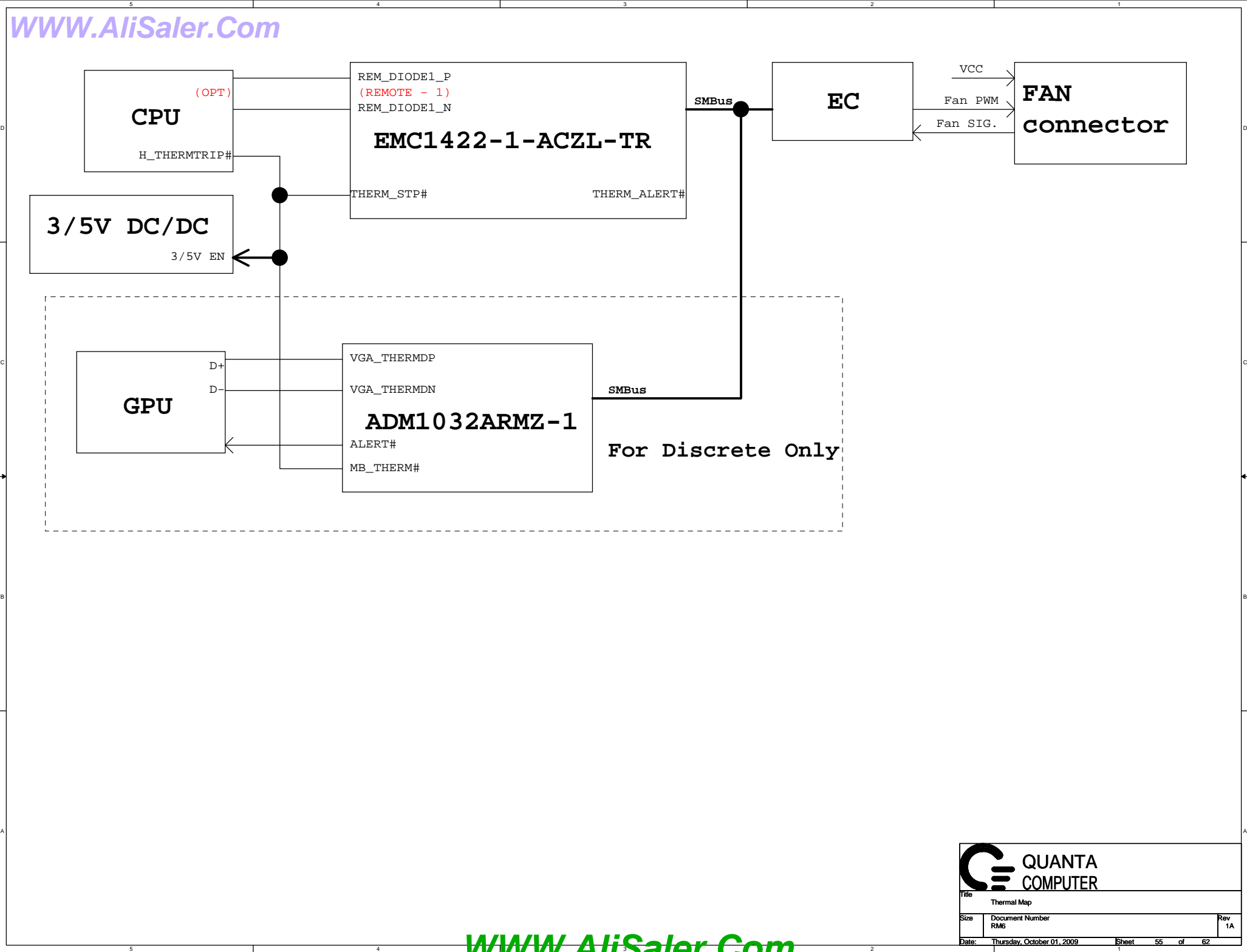
1008 Steg: Add an solder mask between CON1 and screw hole.

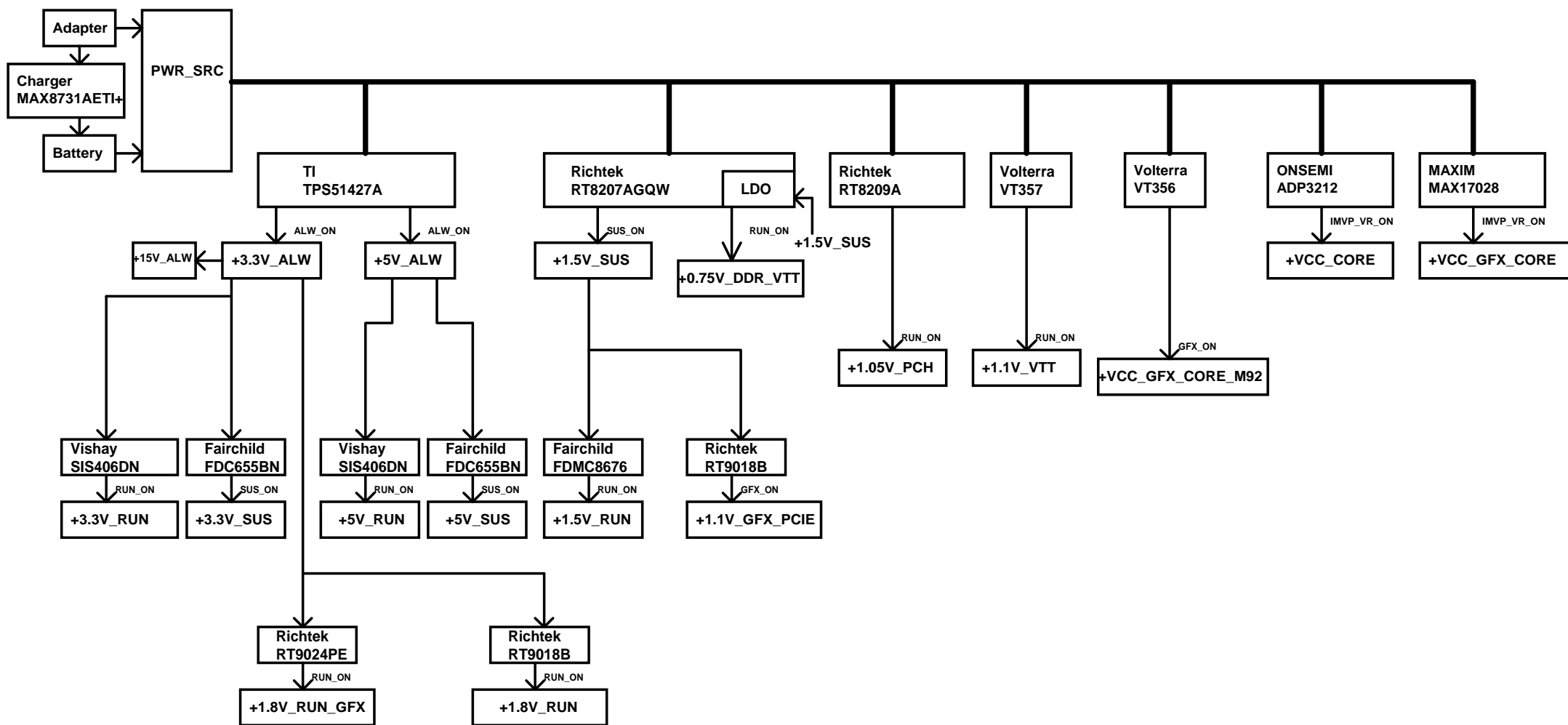


 QUANTA COMPUTER		
Title: SCREW PAD		
Size: RM6	Document Number:	Rev: 1A
Date: Thursday, October 08, 2009	Sheet: 52	of: 62

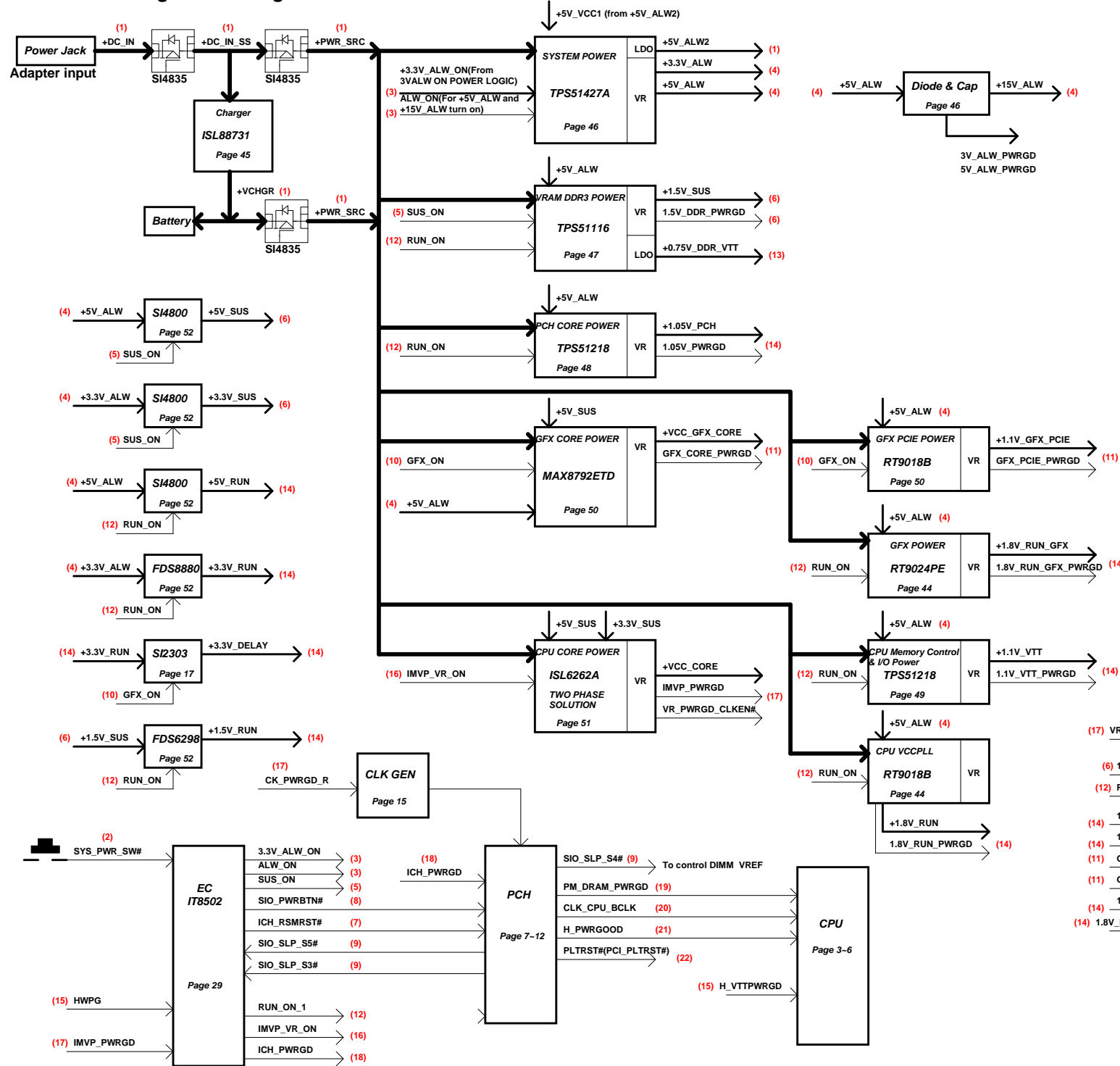
 QUANTA COMPUTER		
Title EMI CAP		
Size RM6	Document Number	Rev 1A
Date: Thursday, October 01, 2009	Sheet 53	of 62



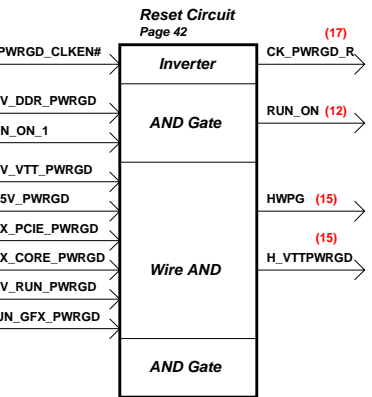




FM9 Power Design Block Diagram 2009/02/25




- (1) AC : DC_IN -> DC_IN_SS -> +PWR_SRC
- (2) Bat : +VCHGR -> +PWR_SRC, +5V_ALW2, SYS_PWR_SW#
- (3) 3.3V_ALW_ON, ALW_ON
- (4) +3.3V_ALW, +5V_ALW, +15V_ALW
- (5) SUS_ON
- (6) +5V_SUS, +3.3V_SUS, +1.5V_SUS, 1.5V_DDR_PWRGD
- (7) ICH_RSMRST#
- (8) SIO_PWRBTN#
- (9) SIO_SLP_S5#, SIO_SLP_S4#, SIO_SLP_S3#
- (10) GFX_ON
- (11) +VCC_GFX_CORE, +1.1V_GFX_PCIE and PWRGD
- (12) RUN_ON_1(RUN_ON)
- (13) +0.75V_DDR_VTT
- (14) +5V_RUN, +3.3V_RUN, +3.3V_DELAY, +1.8V_RUN_GFX, +1.5V_RUN, +1.1V_VTT, +1.05V_PCH ad PWRGD
- (15) IMVP_VR_ON
- (16) +VCC_CORE, IMVP_PWRGD
- (17) ICH_PWRGD
- (18) PM_DRAM_PWRGD
- (19) CLK_CPU_BCLK(PCH to CPU)
- (20) H_PWRGOOD
- (21) PLTRST#(PCI_PLTRST#)
- (22) PLTRST#(PCI_PLTRST#)



1	2	3	4	5	6	7	8	
A								A
B								B
C								C
D								D
1	2	3	4	5	6	7	8	

<



QUANTA
COMPUTER

Title		
SMBUS BLOCK		
Size	Document Number	Rev
RM6		1A
Date:	Thursday, October 01, 2009	Sheet 58 of 62